MODELING, DESIGN, FABRICATION AND CHARACTERIZATION OF POWER DELIVERY NETWORKS AND RESONANCE SUPPRESSION IN DOUBLE-SIDED 3-D GLASS INTERPOSER PACKAGES

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor in Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2015

MODELING, DESIGN, FABRICATION AND CHARACTERIZATION OF POWER DELIVERY NETWORKS AND RESONANCE SUPPRESSION IN DOUBLE-SIDED 3-D GLASS INTERPOSER PACKAGES

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[To my parents, and to my wife]

ACKNOWLEDGEMENTS

First, I would like to thank my thesis advisor Prof. Rao R. Tummala for his support throughout my PhD study. The trust he placed on me to fulfil his research vision at Georgia tech provided the opportunity to pursue my doctoral degree. I also wish to thank Dr. Venky Sundaram, my mentor, for his advice through these years.

I would like to express my sincere gratitude to my committee members: Dr. Sudhakar Yalamanchili, Dr. Joungho Kim, and Dr. Suresh Sitaraman for their guidance to improve my thesis research.

The research and support staff at the packaging research center (PRC) will always be remembered for their professional help. I would like to thank Dr. Raj, Dr. Fuhan, Dr. Vanessa and Mr. Sungjin for useful technical discussions. The help from Jason, Chris, Patricia, Karen and Brian is also highly appreciated.

I would like to thank the member companies of the Silicon and Glass Interposer (SiGI), Low cost Glass Interposers and Packages (LGIP) and Embedded MEMS, Actives and Passives (EMAP) consortium programs. My work at PRC was enriched through the collaboration of numerous hard-working visiting engineers. My special thanks goes to Yoichiro (Asahi Glass Company, Japan), Yuya (Zeon Corporation, Japan), and Furuya (Ushio, Japan).

My stay in Atlanta has been a joyful experience due to my friends. I will always remember their help. Finally, I owe my deepest gratitude to my family. They helped me start and finish this dissertation, and provided selfless support during difficult times. This dissertation is dedicated to my wife.

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SUMMARY

Smart systems require high logic-to-memory bandwidth (BW) with a) lowest power consumption, b) ultra-miniaturized form factor, and c) at lowest cost. Due to the limits of current package-on-package (POP) approaches, 3-D integration has been proposed for improving BW using ultra-short interconnections (30-50μm) at highest I/O density. The targeted 3-D approach of directly stacking logic and memory ICs using Through- Silicon- Vias (TSV), however, leads to design, thermal and infrastructure limitations due to the placement of large, complex and expensive TSVs in the logic die. To address these problems, 3-D glass interposers with Through-Package-Vias (TPVs) at the same pitch as TSVs have been demonstrated as a simpler and superior alternative to direct 3-D stacking of logic and memory devices. Such 3-D interposers provide low-loss, wide-I/O channels between the logic device on one side of the ultra-thin glass interposer and memory stack on the other side, eliminating the need for complex TSVs in the logic die. However, this configuration introduces power delivery network (PDN) design challenges due to resonances arising from (a) added parasitic inductance in the lateral power delivery path from the printed wiring board (PWB), due to die placement on the bottom side of the interposer, and (b) the low-loss property of the glass substrate.

The objective of this research is to model, design and demonstrate effective PDN performance in ultra-thin (30-μm), 3-D double-sided glass BGA packages to achieve high bandwidth, by suppressing the PDN noise from mode resonances. To meet these objectives, this research is organized into three main tasks: a) electrical modeling and fundamental investigation of P/G resonances in 3-D interposer PDN, b) design of

suppression methods to eliminate resonances arising from both the glass substrate and the lateral PDN path, and (c) fabrication and verification of the proposed methods by electrical characterization of ultra-thin glass test vehicles. This research, for the first time, studies the resonance mechanisms in 3-D glass interposer PDN in order to determine the impact of the double-sided logic-memory configuration. Based on this analysis, three important suppression schemes were developed, namely, (a) 3-D interposer package configuration, (b) the selection and placement of decoupling capacitors, and (c) coaxial P/G TPVs. In addition to 3-D glass interposers, the techniques presented in this dissertation can also be applied to the design of single chip 2-D packages and multi-chip 2.5-D glass interposers.

The self-impedance of the 3-D glass interposer PDN was simulated using electromagnetic solvers, including printed-wiring-board (PWB) and chip-level models. A PDN stack-up is introduced with power and ground plane pairs across each build-up in a four-metal-layer glass interposer, to achieve 10X reduction in the inductive impedance. Coaxial TPVs with high dielectric constant thin films between the power and ground via conductors were developed to form ultra-miniaturized decoupling capacitors along the package power path. The impact of design variations on the self-impedance profile was evaluated for variations in die placement, stack-up definition, and the placement of decoupling capacitors. Design guidelines to achieve the target PDN impedance for different applications were formulated through the integration of all the proposed noise suppression methods. Two-metal and four-metal layer test vehicles were fabricated on 30-μm and 100-μm thick panel-based glass substrates respectively, to validate the modeling and analysis of the proposed approach. The PDN test structures were

characterized up to 20 GHz for plane resonances and network impedances, with good model-to-hardware correlation. This research concludes with the electrical characterization and demonstration of PDN resonance suppression in 30μm ultra-thin glass interposers.

The key contributions and novelty of this dissertation can be summarized as follows:

- First demonstration of power integrity for the 3-D glass interposer approach to achieve target impedance for high BW applications
- A simplified method for double-sided power delivery design is introduced using power and ground planes having
    - Ultra-thin 30μm glass cores to mitigate the PDN loop inductance
    - Thick power and ground planes to minimize IR-Drop
    - Multi-layer package stack-up based on panel-based double-side fabrication process for potential lower cost and improved electrical performance.
- Fundamental study of power-ground resonance mechanisms from low dielectric loss substrates in double-sided 3-D BGA packages
- Design and Demonstration of PDN inductance suppression techniques in the 3-D BGA to mitigate resonances from both fundamental challenges
- A new PDN design method based on coaxial power-ground glass TPVs with high dielectric liners with improvement in high frequency resonance suppression
- Electrical design guidelines for 2-D and 3-D glass packages to achieve high BW

CHAPTER 1

INTRODUCTION

Smartphones and tablets continue to drive the need for high bandwidth (BW) between application processor (AP) and memory ICs. Based on JEDEC and industry roadmaps [1, 2], the doubling of data bandwidth occurs each year, similar to Moore's law for transistor scaling [3]. This trend, as illustrated in Figure 1, is projected to increase from 5 GB/s today to an estimated 50-200 GB/s in the next decade [2, 4]. However, such systems continue to shrink in size, imposing additional demands to achieve these bandwidths in smallest form-factor, in addition to lowest cost and lowest power consumption.

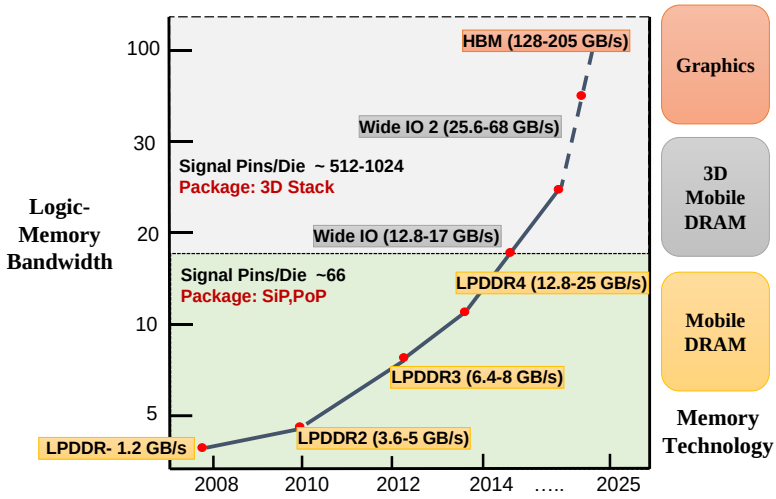


Figure 1: Bandwidth demand in smart mobile systems

At its simplest form, this data bandwidth (unidirectional) can be defined as the product of two factors, namely, the number of interconnections (I/Os) between the ICs, and the signal bit rate per I/O, as shown in Equation 1 [5].

Bandwidth = Number of signal interconnections x Bitrate/pin **Eq. (1)**

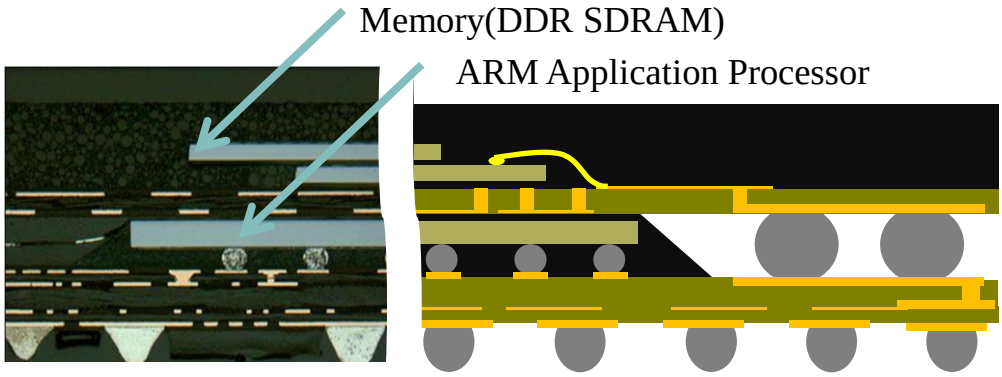


Figure 2: Cross-section of Apple A4 Package-on-Package [6]

Current smartphones are packaged using Package-on-Package (PoP) technology, with wire bonded memory stack packages interconnected by solder joints to packaged logic devices. This configuration, as shown in Figure 2, imposes limitations in achieving the BW due to the long interconnection length (~ 3-5 mm) and low I/O densities (~ 66 I/O) [7]. Consequently, the off-chip I/Os typically require 0.5-5 milli-watts/Gbps of power to drive signals across the lateral package traces with high latency [8]. Therefore, the higher power consumption and long interconnect lengths limit the bandwidth of the PoP to approximately 25 GB/s.

1.1 Technology options for high bandwidth logic-to-memory integration

To meet the demands of continued high bandwidth needs, three interconnection options can be considered [9].

1) 3D ICs with TSVs in Logic IC:

The first approach is the vertical stacking of logic and memory chips, interconnected by Through-Silicon-Vias to form so called 3D-ICs, as shown in

Figure 5(a). This most popular approach to logic-memory stacking, under development, focuses on stacking four DRAM dies bonded Face-to-Back (F2B) on to a logic die at the bottom, interconnected by through-silicon-vias (TSVs). This die stacking method requires TSVs in the logic IC to provide wide I/O channels (500-2500) [10, 11] with high I/O density. The logic-to-memory interconnection length in this approach is reduced to 30-50µm between each ICs enabled by thinning of the dies, resulting in significant reduction in power consumption. This die stack can be then be mounted on silicon, organic or other interposers, fanning out to the printed wiring board (PWB).

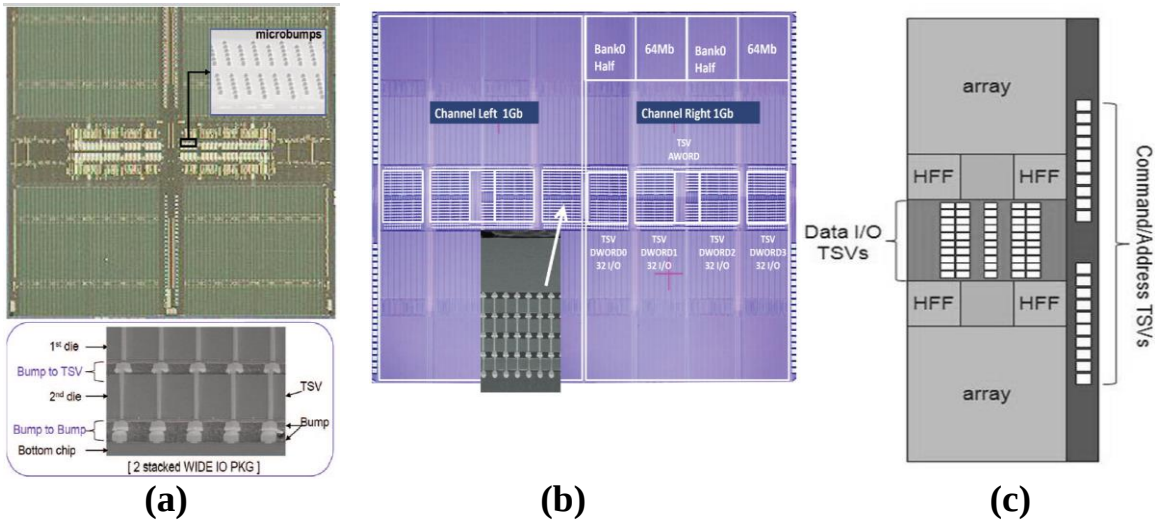


Figure 3: I/O placement arrangement with TSVs connections *(a)* Samsung Mobile wide-I/O DRAM [11], (b) SK Hynix High-Bandwidth-Memory (HBM) [12], and (c) Micron Hybrid-Memory-Cube(HMC) [13]

There has been significant progress in technology development and transition to high volume manufacturing but only in 3-D DRAM memory die stacks using TSVs [14]. However, the current dimensions of TSVs are 5-30X larger than the standard cells in 14-32nm technology. Hence, each section of the memory die is segmented as separate memory banks, leading to increased isolation and yield. Such architecture arrangement

results in the placement of large-size TSV pads in the center of the die stack. As illustrated in Figure 3, memory dies can be efficiently stacked using TSVs due to their regular arrangement of repeating cells. Unfortunately, the same placement of such large TSVs in the logic die can create several drawbacks including: (a) thermal management of logic die within the stack [15], (b) complex co-design requirements between separate logic and memory dies, (c) large mechanical and electrical "Keep-out" Zones due to thermo-mechanical stress on active devices from TSVs, (d) high electrical signal loss and coupling due to the semiconducting nature of the silicon substrate, and (e) testability issues of the die stack without Known-Good-Dies in the stack (KGD) [16]. In addition to these technical challenges, (a) manufacturing and supply chain challenges [17] and (b) the high cost of wafer-based TSV processing [18] prevented wide-spread adoption of 3D logic-memory stacking so far.

Therefore, these cost, thermal and other above challenges associated with 3D IC stacking have created a strong need to explore and demonstrate alternate approaches to enable high logic-to-memory bandwidth, without the use of TSVs in logic ICs.

2) 2.5D interposers with passive silicon interposers:

To overcome the above challenges due to TSVs in logic dies, a second approach was developed, using multichip modules (MCMs) with side-by-side interconnections between logic chip and 3D memory stacks. This approach can be viewed as being similar to IBM's multi-chip-modules (MCM) in the 1980's fabricated out of package foundry in contrast to the new approach that produces MCM with wafer BEOL processes, with much higher I/O density and is termed as 2.5D interposer [19-22]. Logic-to-memory interconnections are achieved with multiple layers of ultra-fine re-distribution layers

(RDL) on passive silicon interposers, and employs TSVs only in the Si interposer to connect to the organic BGA package, thus eliminating the need for TSVs in the logic chip. These 2.5D interposers also provide additional benefits in design flexibility, scalability, testability and thermal management. This configuration, as shown in Figure 4, has been demonstrated and manufactured to connect multiple FPGA slices [23] and FPGA cores with High-Bandwidth-Memory. However, this 2.5D approach presents challenges from longer lateral signal interconnections [24] and the very high cost of the silicon interposers. The high cost is attributed to the small number of interposers produced from 300 mm wafer, in addition to the expensive process of TSV formation as well as the wafer-based single-side process for fabricating the redistribution layers (RDLs). In addition, there are added costs due to the need for a separate organic package and its assembly between the interposer and the PWB. . Therefore, an ideal solution should be lower total cost to achieve the bandwidth, including interposer cost, assembly and test costs.

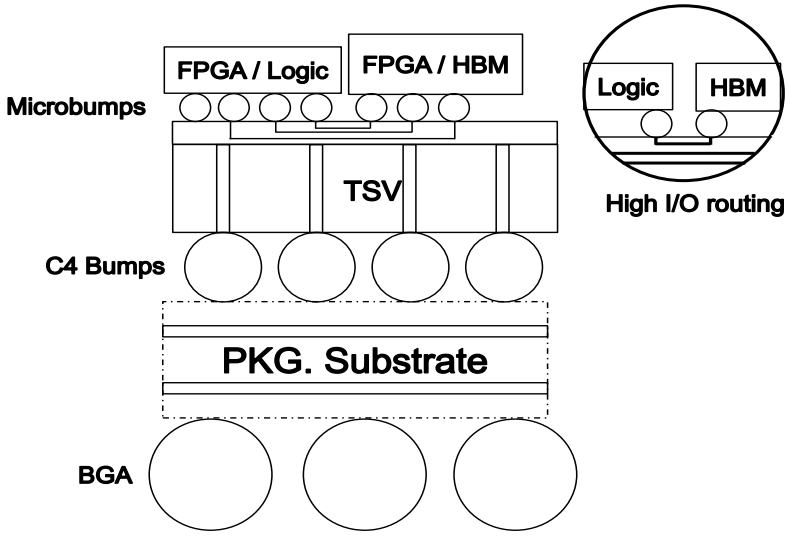


Figure 4: MCM (2.5D) approach with lateral I/O connections using Passive Si interposers

3) 3-D interposer BGA package:

A third and simpler approach, called the 3D interposer package, is proposed here in this thesis project, as a compelling alternative to 3D ICs with TSV and 2.5D Interposers. Such a concept is three-dimensional, does not require TSVs in logic ICs, and separates logic from the memory stack by assembling logic IC on one side and memory stack on the other side of an ultra-thin interposer made out of ultra-low loss glass with through-package-vias (TPVs) at the same I/O density as TSVs in 3D ICs. Moreover, unlike Si interposers that require an additional organic package for interconnection to the system board, the new 3-D interposer BGA package is proposed to be attached directly onto the printed wiring board (PWB) through standard SMT interconnections.

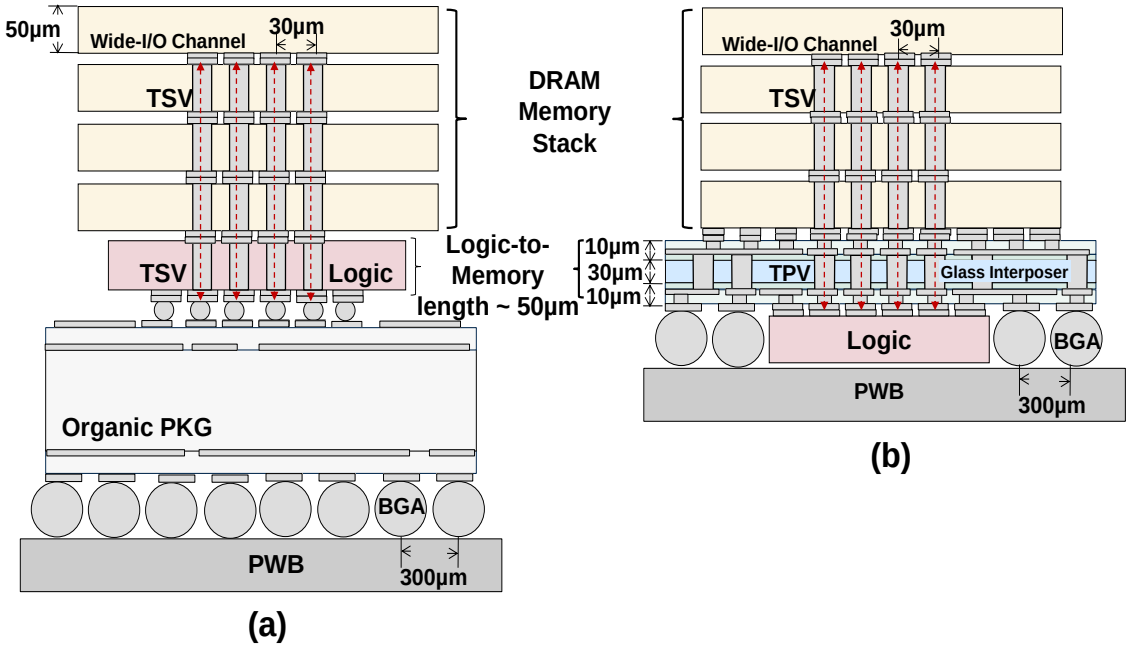


Figure 5: a) 3-D ICs vs. b) 3-D interposers

The three approaches to high bandwidth are compared in Table 1 for relative cost. As shown in Figure 5 (b), the 3-D interposer approach combines the best attributes of the other two approaches to achieve highest bandwidth. Based on these parameters, cost/bandwidth trade-offs associated with different mobile memory technologies are plotted in Figure 6.

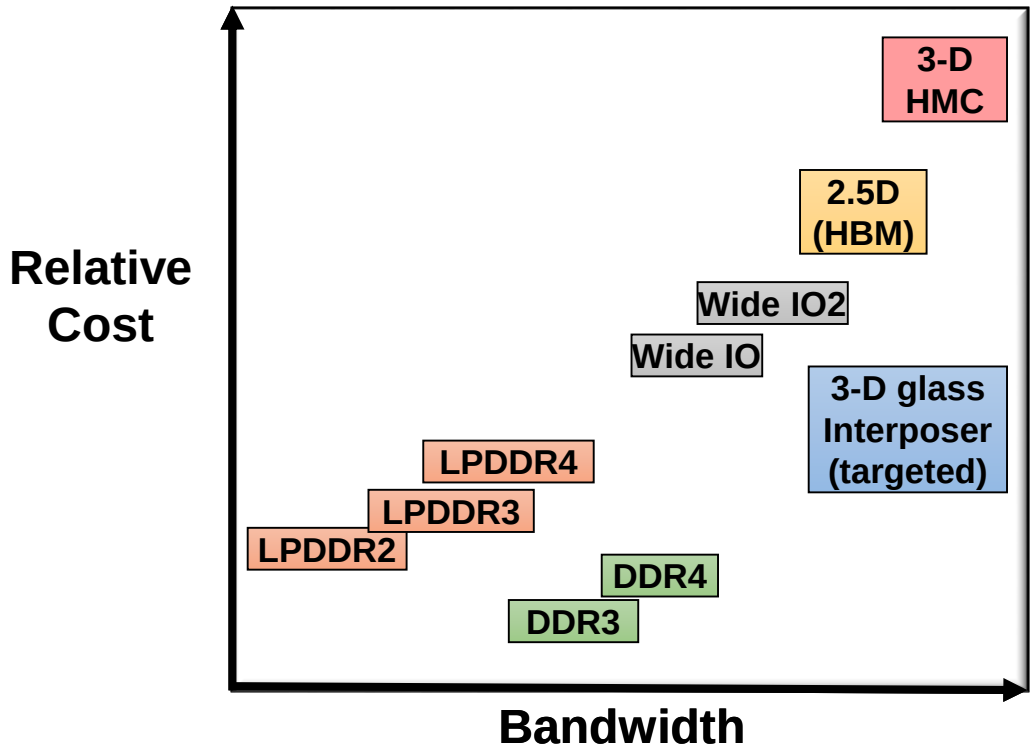


Figure 6: Comparison of various high BW memory integration approaches

Table 1: Comparison between 3D ICs, 2.5D and 3-D Interposer Approaches

Parameters	3-D ICs	2.5D	3-D Interposer
1. Design Flow	Logic-Memory Co-Design required	More design flexibility	More design flexibility

Table 1: Continued

2. Logic Device Impact	Stress from TSVs, TSV keep-out zone required	No impact due to passive TSVs	No impact due to TPVs in package
3. I/O Signal Loss	Small due to short TSV distance (50µm)	Medium to High due to Lateral I/O on thin oxide liner	Lowest loss due to insulating substrate material and short TPV distance (50µm)
4. Power Delivery Impedance	Medium to High due to small multi-die 3-D IC footprint	Existing Package Design Applicable	**Challenging due to BGA reduction and low-loss substrate (focus of this thesis)**
5. Testability	KGD requirement for both logic and memory stack	May require KGD based on assembly yield	Intermediate testability for higher yield
7. Thermal solution	Challenging	Existing package thermal solutions can be adapted	Thermal isolation of logic from memory stack due to insulating glass
6. Relative Cost	High cost due to • High process complexity • Infrastructure challenges	High cost due to • Small wafer size, up to 300 mm • Costly TSV and BEOL process	Lower cost due to • Cheaper raw material • Large panel size, up to 700 mm • Simpler double-side process with reduced steps

1.2 Rationale for 3-D Glass BGA Interposer Packages

A 3D interposer is defined as a 3D stack of two or more logic or memory ICs interconnected by shortest interconnect length between logic and memory, and assembled on both sides of an ultra-thin interposer. This method enables ultra-short interconnections similar to 3D ICs with TSVs, but without the need for TSVs in the logic chip, in addition to improved thermal and cost benefits than the other two approaches. In this approach,

the interposer substrate proposed is made up of ultra-thin glass in contrast to, silicon, or organic substrates. Glass is proposed and studied as the best electronic substrate material for 3D interposers in this dissertation due to its numerous advantages that include lowest electrical loss and lowest cost due to large area processing[25]. In addition, there has been significant progress with the fabrication of ultra-thin glass substrate at Georgia Tech PRC with its industry consortium to enable the high-speed formation and metallization of ultra-fine-pitch TPVs.

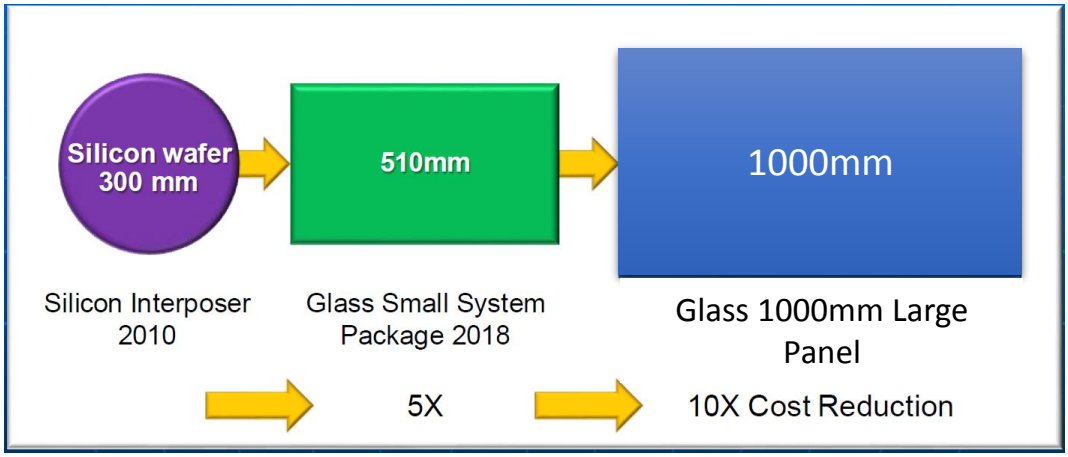


Figure 7: Low cost of Glass is due to large panel processing (Prof.Tummala)

Glass is an excellent insulator; it is thermally and dimensionally stable; it has smooth surface, thus enabling very low signal loss and coupling [26], and is proposed to be fabricated with very high I/O density, similar to TSVs in Si. Further, glass substrates can be processed as large panels upto and beyond 510 mm in size, resulting in lower cost by an estimated factor of 5-10X over wafer-based BEOL silicon interposers [27, 28]. Glass is available as fabricated into ultra-thin sheets (30-100μm) using fusion draw and down draw methods, eliminating the need for expensive chemical-mechanical-polishing

(CMP) in silicon substrates. This vision towards lower cost manufacturing is illustrated in Figure 7. In addition, glass is a thermally stable inorganic material, similar to Si, with high modulus and high-temperature stability. These properties make glass an ideal substrate material for 3-D interposer packages. The material and fabrication advantages of glass substrates over organic and silicon substrates has been reported [29].

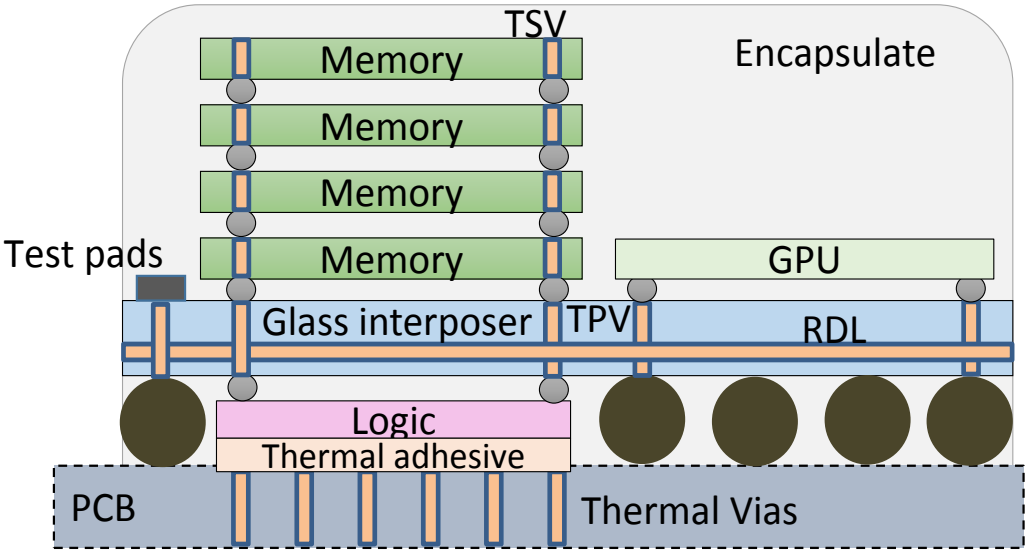


Figure 8: 3-D glass interposer BGA package with multiple dies

While the concept of through vias and double-side assembly has been previously reported for both organic and silicon interposers [30, 31], the proposed 3D glass interposer package approach achieves the ultimate bandwidth performance due to: 1) the same, high I/O density as TSVs in 3D ICs, 2) ultra-short interconnections enabled by ultra-thin glass, and 3) ultra-low electrical loss, characteristic of most types of glass materials. In addition to enabling high logic-to-memory bandwidth, this unique 3-D interposer package concept promises many advantages that include design flexibility, testability, thermal management, and extendability to multi-die applications as shown in Figure 8.

Although this configuration provides a number of advantages, the 3-D double-sided glass configuration introduces fundamental problems in achieving a low impedance power delivery network (PDN). The power delivery design becomes challenging due to the placement of dies at the bottom of the interposer, leading to additional parasitic inductance. This necessitates the use of power and ground planes on the glass substrate to provide the lowest possible impedance. However, the resulting resonances from plane cavities create local maxima above the targeted impedance, which severely affect the voltage and timing margins of high-speed digital circuits. Consequently, careful PDN design is necessary to ensure high BW in 3-D glass interposers.

1.3 Research Objectives and Challenges

The objective of this research is to study, explore and demonstrate effective PDN in ultra-thin (30-µm), 3-D double-sided glass interposer BGA packages to achieve high BW, by suppressing the PDN noise from mode resonances.

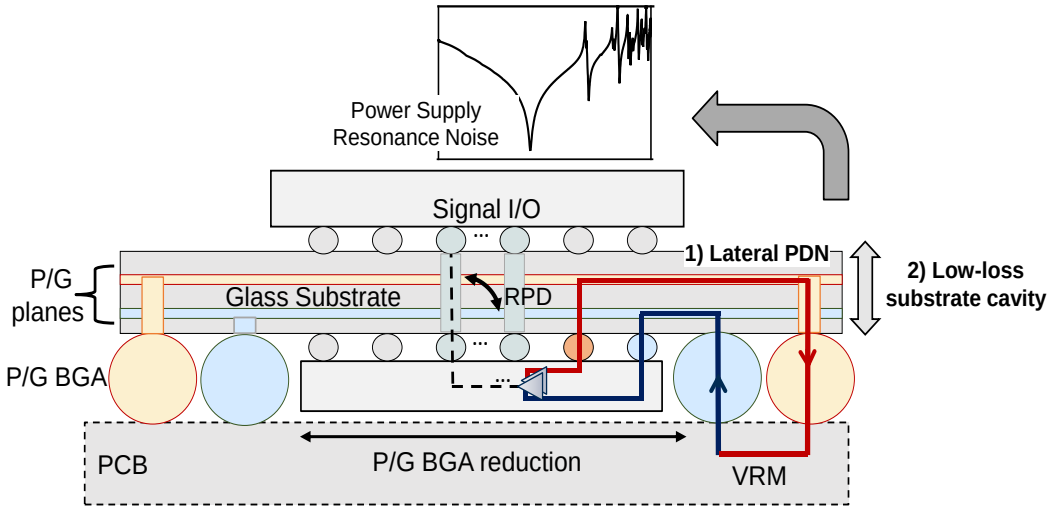


Figure 9: Fundamental PDN challenges with 3D glass interposer BGA package

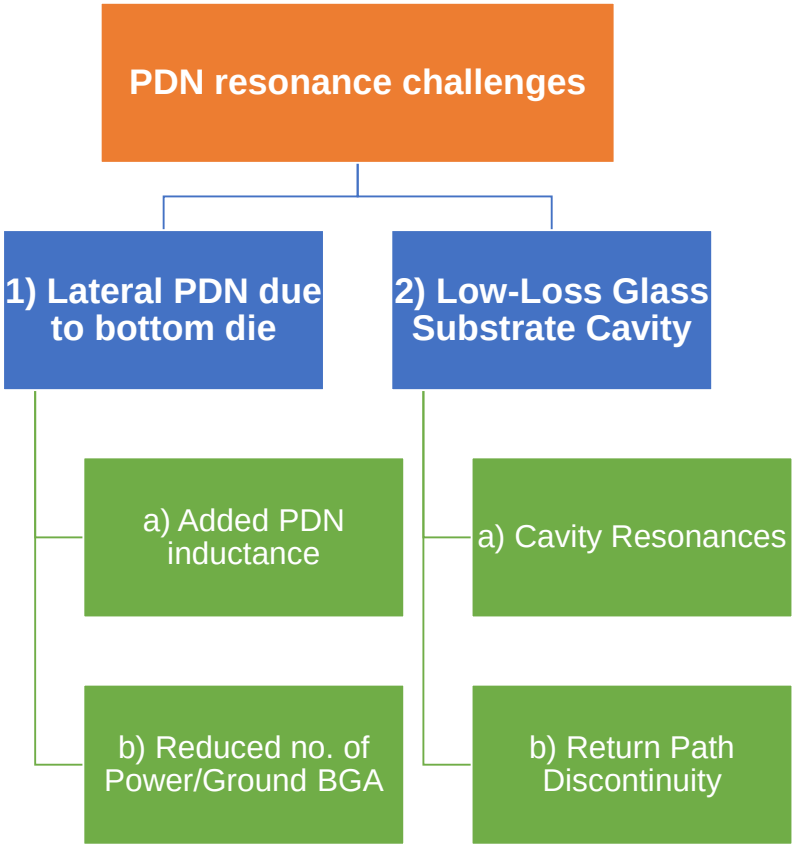


Figure 10: PDN Design Challenges from 3-D interposers

1.3.1 Fundamental PDN Challenges in 3-D Glass Interposer BGA packages

The electrical design of 3-D glass interposer BGA packages imposes significant challenges in achieving low impedance PDN, which leads to associated power and signal integrity problems. These challenges manifest themselves through the increased magnitude and number of resonant peaks in the PDN impedance profile, as illustrated in Figure 9. This impedance variation results in rapid voltage fluctuations at high current densities, and increased simultaneous switching noise (SSN). The associated issues, due to return path discontinuities (RPD), cross-talk, signal-to-power coupling, among others,

present significant obstacles in achieving high BW. Hence, this dissertation primarily focuses on fundamental understanding of the PDN resonances and proposes solutions to address this challenge, due to its critical importance in enabling clean power delivery.

The primary challenges in PDN design of 3-D glass interposer BGA packages can be attributed to two factors summarized in Figure 10:

(1) Power delivery network due to long interconnect length due to underside die placement

(2) Low-loss property of the glass substrate material

The resulting PDN attributes due to each of these challenges are presented in below:

(1) <u>Challenges from Lateral PDN due to bottom die placement</u>

The placement of the die at the underside of the package results in additional PDN parasitic inductance. Fast current switching transients flowing across these parasitic inductances induce very large voltage fluctuations during the device operation. This effect can be correlated to resonances in the frequency domain resulting in overall poor system performance. The additional inductance arises due to two separate but connected reasons as shown in Eq. (2).

$$\begin{matrix}\textbf{Additional} \\ \textbf{3-D interposer PDN} \\ \textbf{Inductance}\end{matrix} = \textbf{Lateral trace inductance} + \begin{matrix}\textbf{Added BGA} \\ \textbf{interconnect} \\ \textbf{inductance}\end{matrix}$$

Eq. (2)

i. Lateral Power Delivery Path

The placement of logic or memory dies on the underside of the 3-D interposer package results in the inability to connect the ICs mounted on the interposer directly to the PWB using centrally-placed power-ground (P/G) TPVs. Hence, this configuration creates additional PDN inductance due to a much longer (3-5mm) lateral power delivery path. Moreover, the placement of land-side capacitors at the center of the package underside also becomes restricted.

ii. Reduction in the number of P/G BGAs

The bottom side die placement decreases the area available for BGA interconnections between the package and the board. Hence, there is a reduction in the total number of power and ground (P/G) BGAs at the center of 3-D interposer packages when compared to a 2D MCM glass package with fully-populated area-array of BGAs. Since the number of signal BGAs are pre-defined by architecture requirements, the total number of P/G BGA's will be reduced in this approach. Depending on the interposer dimensions, this can lead to a loss of 30-50% of P/G BGA's over a 2-D BGA structure. There is a corresponding increase in the current to be delivered to the 3-D dies on the interposer. These factors contribute to additional P/G BGA interconnect inductance arising from a reduction in the number of parallel BGA interconnects.

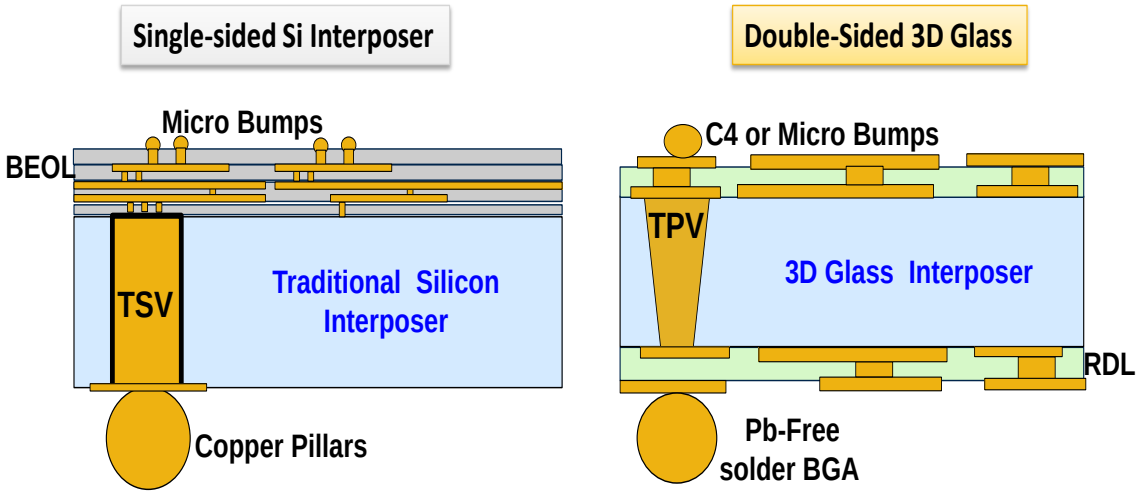


Figure 11: 3D Si BEOL Interposers vs. 3D Glass BGA Interposers

1.3.1.1 Rationale for using Power and Ground Planes in 3-D BGA glass packages

To mitigate the total PDN inductance modeled in 3-D glass interposer packages, solid power and ground planes were designed to achieve the lowest possible impedance. Figure 11 compares the PDN structure of single-sided Si interposer with the double-sided 3-D glass interposer packages. This arrangement provides the following design advantages over P/G traces on the interposer.

1. Reduction of overall P/G loop inductance from the lateral power delivery due to tightly-coupled forward and return current paths.
2. Increased overall higher frequency capacitance due to ultra-thin (30um) glass core
3. Reduction in the Resistive IR-drop due to 5-8um copper thickness

Hence, the approach with solid planes constitutes a fundamental design element in the 3-D glass-interposer PDN.

(2) Challenges from low dielectric loss of the glass substrate

The presence of power and ground planes across a low-loss glass or any other low loss substrates generates cavity resonances at certain frequencies. The severity of the resonances is further increased due to the effects of lateral PDN. The presence of high I/O channels also induces power supply noise and coupling between the signal distribution network and power delivery network. These effects are examined in this sub-section.

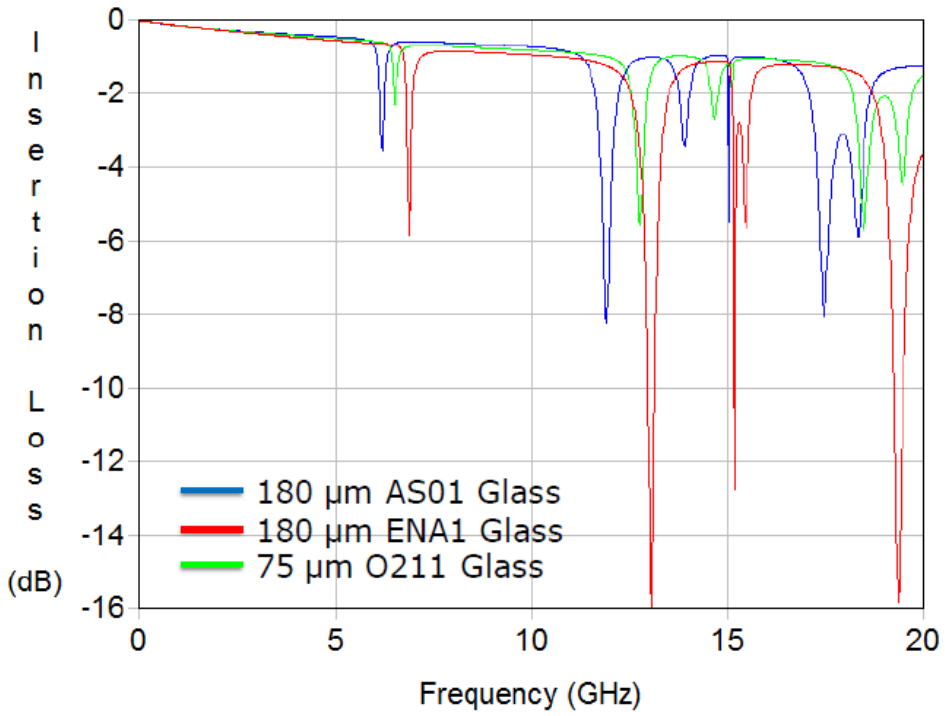


Figure 12: Insertion loss plots of MSL-TPV transitions from [32]

A) Power and ground Cavity resonances

Power-ground planes in 3D double-side glass substrates generate multi-mode cavity resonances due to their high resistivity properties, similar to organic packages. The effect

of P/G resonances has been extensively studied in literature [33], [34]. In contrast to the single-sided silicon interposer, P/G planes form electromagnetic resonating cavities that cause standing waves at microwave frequencies. This spatial variation in the impedance at specific frequency modes generates multi-mode plane resonances. Hence, decoupling techniques are necessary to mitigate this effect.

B) Return Path Discontinuities

The power noise observed due to this effect also causes the degradation of signal insertion loss and noise coupling at resonance frequencies. The impact of signal return path discontinuity is illustrated for different glass thicknesses and materials in Figure 12 from [32]. The effects of noise coupling between signal nets and power/ground planes at resonant frequencies, including the impact of signal return path discontinuity, have also been studied [35]. Hence, careful design of high-density I/O signals with through-via transitions is necessary to achieve signal and power integrity.

1.4 Research Tasks and Organization

This research is organized into three main research tasks based on the fundamental challenges described earlier.

1) Electrical modeling and the fundamental investigation of P/G resonances in 3-D glass interposers
2) Design of suppression methods to eliminate resonances arising from both the glass as a highly insulating substrate material and the lateral PDN path, and
3) Fabrication and verification of the proposed methods, from ultra-thin glass test vehicles

This dissertation document is divided into six main chapters. The introduction to 3-D glass interposers as the best approach to achieve the desired bandwidth is presented in Chapter 1. The fundamental problems due to the proposed approach are also presented, leading to a set of research objectives and tasks. A brief overview of the previously-published background material relevant to this proposal is provided in Chapter 2. A thorough investigation of PDN impact due to the 3-D interposer structure is examined and compared with 2-D MCM glass packages, in Chapter 3. The associated impact on the signal path is also analyzed. Different PDN design techniques to suppress PDN resonances are proposed and designed in Chapter 4. The fabrication and characterization of the test vehicles in demonstration of PDN in 3D interposer are presented in Chapter 5. The final chapter, Chapter 6, summarizes the key contributions and future extensions.

CHAPTER 2

LITERATURE SURVEY

The previous chapter introduced the concept of 3-D glass interposers for high bandwidth logic-to-memory interconnections, and defined the research objectives for this dissertation. Power delivery network resonances (PDN) were identified as the main technical challenge towards achieving high BW in 3D glass interposers, and the primary research tasks to address this challenge were described. This chapter presents a comprehensive review of the published literature relevant to this research, and is organized into three major sections. The first section reviews packaging methods developed for high bandwidth logic-memory integration, with specific emphasis on double-sided interposers. The second section presents recent work on the electrical modeling and high frequency electrical characterization of ultra-thin glass interposers. The final section summarizes important design techniques developed to suppress PDN resonances, including the placement of power and ground BGA interconnections.

2.1 DOUBLE-SIDED LOGIC-TO-MEMORY INTEGRATION

Various direct chip stacking and 3-D interposer integration methods have been pursued in the past few decades to improve bandwidth, reduce power consumption, and achieve system miniaturization [36]. This section focuses primarily on logic-to-memory high bandwidth 3D integration methods without the use of TSVs in the logic ICs.

a) Chip-to-Chip Face-to-Face Bonding:

The simplest 3-D integration solution without the use of TSVs in logic is by Face-to-Face (F2F) die stacking. Direct face-to-face (F2F) bonding between logic and memory

dies were demonstrated using extremely thin ICs (~20µm) in a chip-on-chip (CoC) configuration with limited external I/O connections through wire bonds [37]. Chip-to-wafer bonding was used to increase yield and accommodate the large die sizes. This approach required a complete co-design of logic and memory to match the I/O locations on both dies.

To overcome the limitations of F2F due to wire-bonding, the approach has been extended to multiple dies using flip-chip connections. Multiple smaller dies (daughter) at 30-80µm pitch were connected to a larger IC (mother) to achieve a larger number of die-to-die connections by Amkor [38] to achieve a Chip-on-Chip package (CoC/F2F) as shown in Figure 13. This method has recently received widespread interest due to the simplified stacking process. Reliability tests were also performed on a 40µm thin daughter die connected by 40µm micro-bumps to a 200µm thick mother die in an A-STAR research program [39].

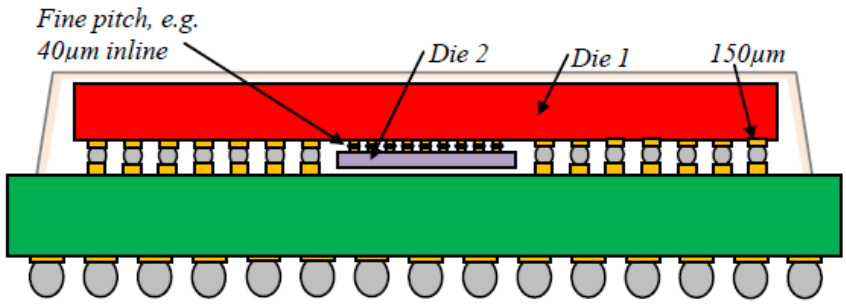


Figure 13: Chip-on-Chip Double-sided approach developed by AMKOR from [40]

This configuration has also been extended for stacked Field Programmable Gate Array (FPGA) applications by Altera [41]. Due to the stacked die space constraints, RDL with ~2 to 3mm routing length was used to fan out and get access to the substrate bumps. Thermal and electrical performance validations were performed to ensure functionality.

Power integrity was identified as a critical design challenge due to the larger IR-drop and resistance values from very thin and narrow RDL traces, as a result of wafer back end of line (BEOL) process limitations. However, this effect had lower resonance peak magnitude when compared to a conventional flip-chip package as shown in Figure 14. In this approach, careful PDN design is required to balance the desired DC and high frequency target impedances. In addition, this integration faces significant challenges due to die thinning, scalability, high cost and co-design problems that limit its effectiveness for high BW applications.

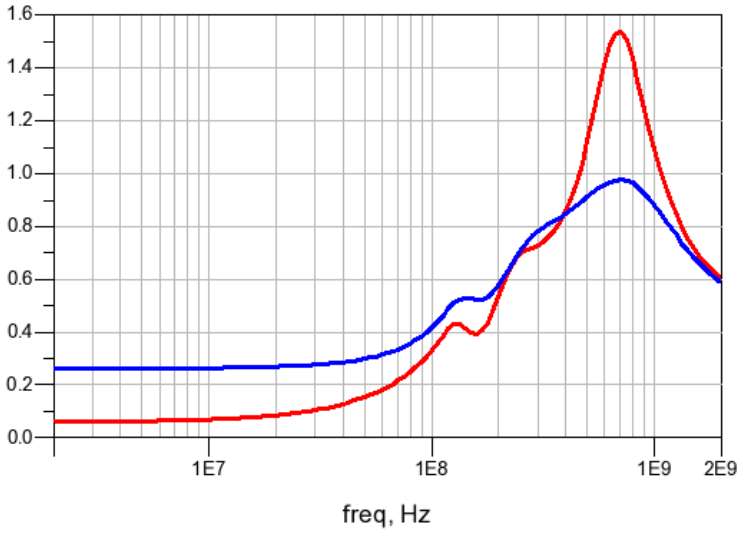


Figure 14: PDN impedance comparison between conventional package and F2F package [41]

In order to overcome the challenges of direct face-to-face stacking, passive interposers with double-side die attachments have been developed to provide improved design flexibility for integrating dies with different I/O footprints. This 3D interposer approach also provides cost-effective, high performance interconnections between multiple chips on either side.

b) Organic substrate-based double-sided Integration:

The use of conventional organic packages as double-side die substrates was originally developed to allow direct surface mount technology (SMT) assembly to printed wiring boards. The first double-sided stacking of logic and memory was developed by NEC for mainframe applications in early 1990s. It used a SMT package stacking method to provide high I/O interconnections between LSI chips as shown in Figure 15 [42]. For logic-to-memory integration, researchers at NEC proposed and demonstrated a 3D package using an organic feed-through-interposer (FTI) [30, 43]. Logic and eight-chip memory stacks were mounted on both sides of the FTI with 50 µm-pitch flip-chip connections. Device operation at 3-Gbps was demonstrated with prototype DRAM and LSI integration. Due to the I/O density limits of the FTI substrate, NEC later also adopted a wafer processed silicon interposers for double-side logic and memory integration, as described in Figure 16. Assembly, reliability and thermal cycling studies were also performed [44, 45].

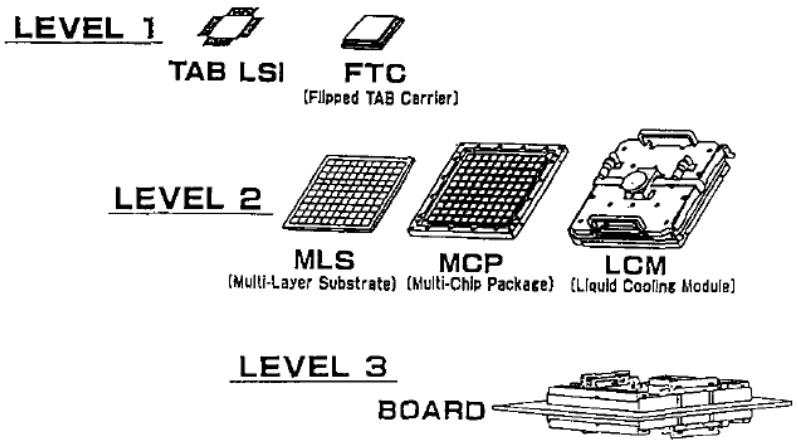


Figure 15: Double-sided SMT organic package stacking for high logic-memory BW from NEC in 1992 [42]

This technology was applied to Network-on-chip applications (3D-NOC) at NEC using two homogenous dies connected through an organic interposer [46]. Significant benefits were obtained due to the ability to fabricate multiple RDL wiring layers beyond the limits of TSV and C2C technologies. Though-interposer-vias in organic substrates were used at 150µm pitch to provide die-to-die connections with very low signal loss and coupling.

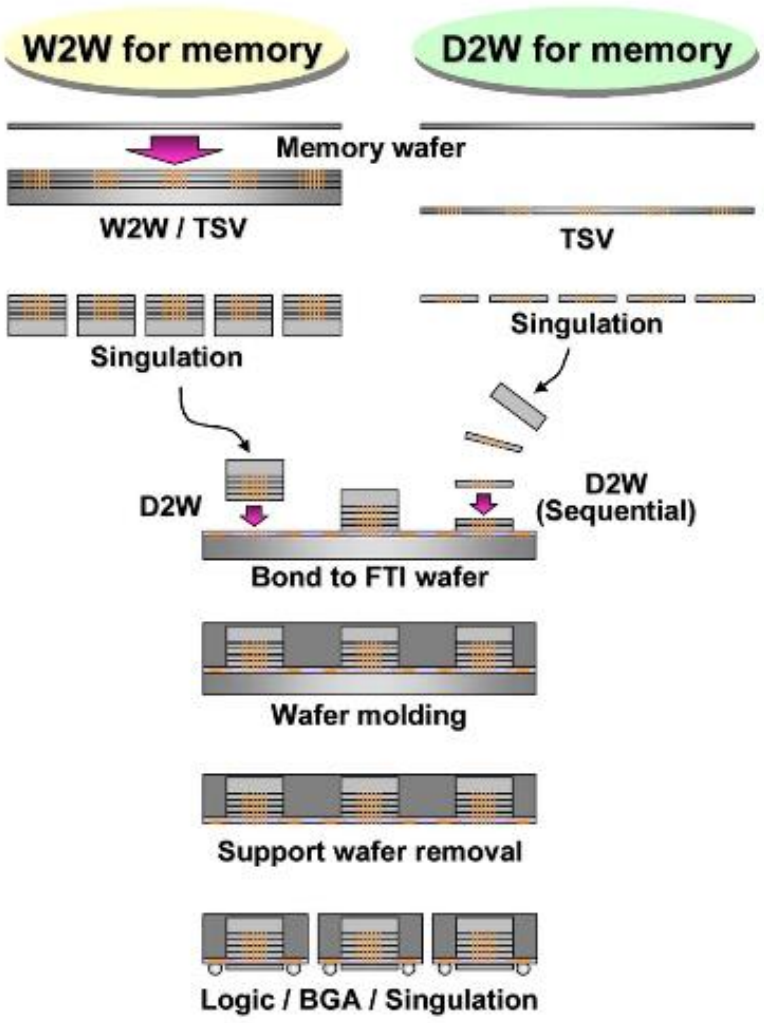


Figure 16: Double-sided 3-D organic package logic-to-memory integration using SMArt Feed Through Interposer (SMAFTI) technology [30]

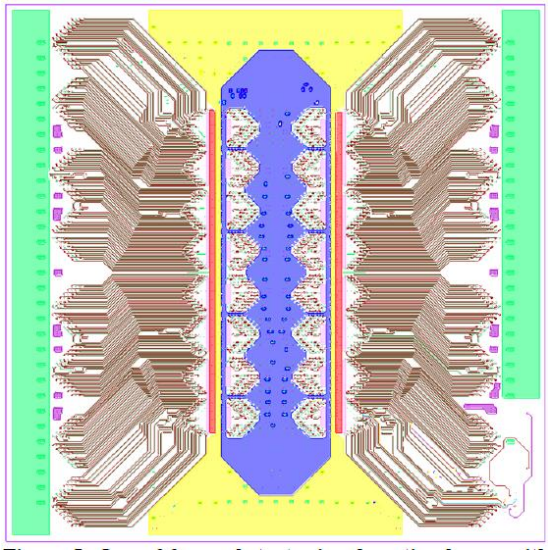


Figure 17: Power Planes in double-sided organic package from Rambus [47]

A similar double-sided organic package approach was applied to integrate DRAM stacks with memory controllers using multiple RDL layers for chip-to-chip interconnections [47-49]. A 512 bit wide memory interface was routed to a logic controller die to achieve an aggregate peak bandwidth of 256GB/s with 40W peak power. The details of signal insertion loss modeling and package escape routing were presented. The power delivery challenges with the double-sided configuration were briefly discussed, along with a pre-layout design strategy. Multiple power and ground islands were employed to provide the lowest PDN impedance. The PDN design was optimized across 11 power domains due to the stringent impedance target requirements. IR drop and PDN inductance (12-200 pH) were quantified for different power supply rails. While this method addresses the challenges of TSV in logic, they are still limited by the through-package-via pitch (>100µm) and wiring (>8-10 µm) features in organic build-up substrates.

c) Silicon-based double-sided Integration:

Silicon interposer based 3D SiPs have been developed to meet high I/O requirements beyond organic interposers, with 5-10 μm diameter through-vias between the memory and logic dies [50], [51]. The double-sided silicon interposer was fabricated with a size of 18mm x 18mm and a thickness of 100μm, on a 300mm Si wafer, and the TSV diameter was 10μm. This method provided much higher wiring density than organic substrates, due to BEOL IC fabrication processes. Contact aligners were used for all lithographic processes. The RDL fabrication was done using modified double-sided Cu-damascene processes. The process flow for the final assembly of multiple dies was developed, where the sequential reflow and under filling was performed for each die before solder ball mounting. VNA characterization was also performed to quantify the electrical performance of the passive test structures.

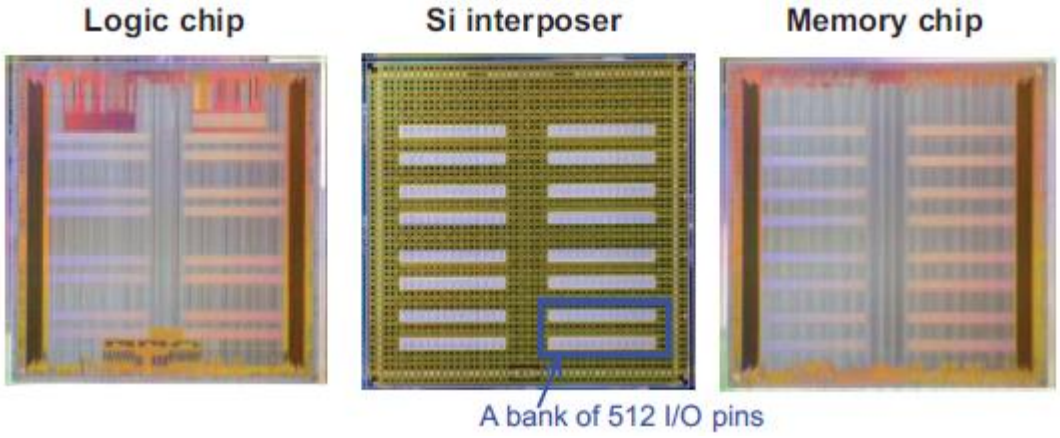


Figure 18: Layout of Passive Si Interposer with double-side logic and memory dies from [51]

To study the power distribution network (PDN) impedance and simultaneous switching output (SSO) noise characteristics of such 3D interposers, a 4096 bits wide-bus

device using interposer through-silicon-vias (TSVs) was designed and fabricated [31]. The anti-resonance peak of total PDN impedance was extracted at around 80 MHz, with a maximum SSO frequency of 75 MHz A phase-clocking scheme was also implemented to reduce the switching current noise.

Although silicon interposers meet the high I/O requirements required for achieving high BW, the TSVs suffer from (a) high electrical loss due to the semiconducting nature of the silicon substrate, (b) high cost due to small wafer size and complex TSV and RDL fabrication processes, and (c) interposer-to-organic PWB CTE mismatch. To address the cost and electrical performance barriers of wafer-based silicon interposers, a panel-silicon approach using poly-crystalline silicon was demonstrated with lower loss due to thick organic liners [52]. The prior art in silicon and organic double-sided interposer integration schemes is summarized in Table 2.

Table 2: Summary of double-sided interposer integration approaches

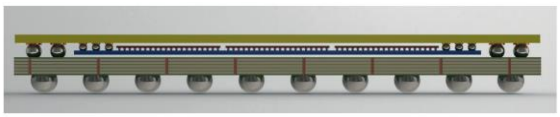
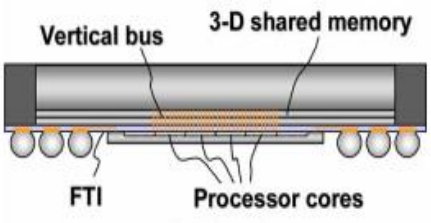
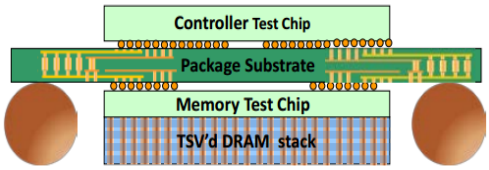
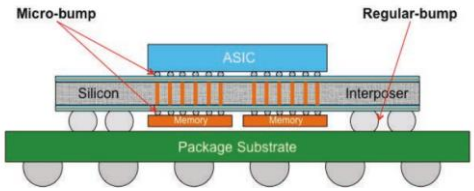
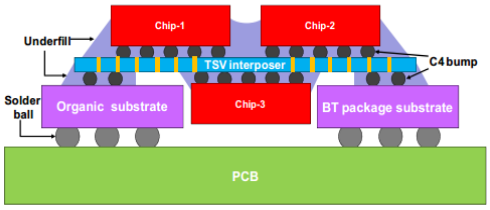
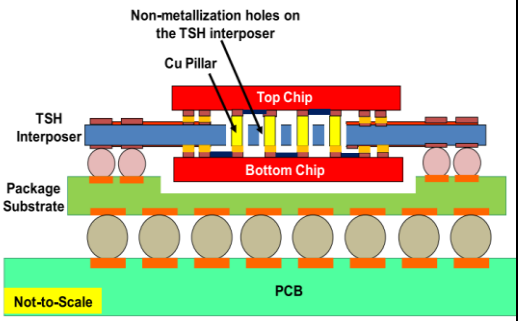
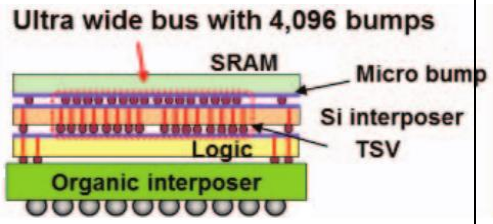
Ref.	Configuration	Description
[38]		• Multi-Chip stacking alternative • Chip on Chip, Face to Face connections with flip-chip
[43]		• Organic interposer (33x33 mm^2) with Si wafer carrier • First level Through-package-via pitch (50µm) and wiring (5 µm) • 1mm second level, 520 balls

Table 2: Continued

[47, 48]		• 35x35mm^2 Organic Package • 1600 signal nets at 4 Gbps • 5/2/5 Buildup, 400-µm core • 256 GB/s BW between memory and controller dies
[31]		• Si Interposer 28 x 28 x 0.15 mm^3 • DRIE based TSVs • 1 logic + 2 Memory integration • 256-512 I/Os
[50]		• 100µm-thick Si interposer with 10µm-diameter TSVs • 3 RDLs on its front-side with 2 chips on top • 2 RDLs on its backside with 1 die mounted at bottom
[53]		• 15-µm Through-Silicon-hole via with lower loss than TSVs • 5x5mm^2 Top chip and Bottom Chip on 10x10 mm^2 Si interposer • 15x15 mm^2 packaging organic substrate • 6x6x0.5 mm^3 Cavity in the organic substrate to place bottom chip • 100- µm FLI copper pillar
[51]		• 3D SiP with Silicon Interposer • 4K I/O (8x 512 channel) between logic and memory • 19-36% SSO noise reduction by phase-shift clock technique

2.2 ELECTRICAL DESIGN OF GLASS INTERPOSERS

The novelty of this research is in the use of ultra-thin glass interposers for 3D logic-to-memory integration, addressing the limitations of organic and silicon interposers discussed in the previous section. This section discusses the published research in the electrical design of glass interposers. Previous interposer design research has primarily focused on passive silicon interposers with TSVs. These interposers suffer from high signal loss and cross-talk due to the inherent semiconducting nature of the silicon substrate. Glass interposers address the cost, electrical performance and reliability limits of silicon interposers as well as the I/O limits of organic substrates [25]. Hence, the electrical design of glass substrates as interposers has received much attention in the recent past due to its low-loss properties, with most published work focusing on signal integrity.

A preliminary study of insertion loss and cross-talk in 200-500 µm glass wafers having for 400µm pitch tungsten vias was performed using electromagnetic solvers [54-56]. Initial studies on high frequency behavior of Through-Glass-Vias (TGVs) with copper vias were investigated for RF applications [57]. Sukumaran et al, [58-60] examined the design, fabrication and characterization of glass as an interposer material, focusing on TPV formation and metallization. Electromagnetic modeling and design of through package vias (TPVs) in glass were discussed in detail, and the feasibility of 50-µm pitch TPVs in 180-µm thin glass substrates demonstrated. Simulations were performed for Glass TPVs with different dimensions and polymer material combination to study the signal loss and crosstalk [32]. In addition, initial studies on glass TPVs connected with CPW-RDL transitions were presented. Recent research on contact-less

electical interconnections observed that bump-less high speed channel on organic and glass interposer shows better electrical performance compared to silicon interposer[61].

Glass as an interposer faces electrical design challenges, mainly in the design of power delivery networks (PDN). The high impedance of multi-layer glass substrates generates multi-mode plane resonances that are common to all high-resistivity substrates including organic packages. The resulting power noise causes degradation of signal insertion loss and noise coupling at resonance frequencies. This effect has extensively been studied in the past decade [33], [34] and is illustrated for different glass thickness and materials in Figure 19 from [32].

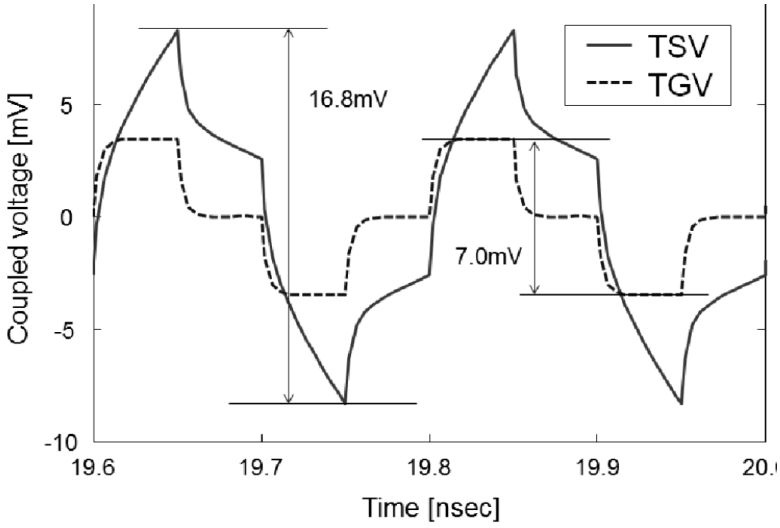


Figure 19: Near-End coupling comparison between TSVs and TPVs from [26]

In recent work, the electrical characteristics of glass interposer PDN were analyzed and compared with silicon interposers. The effects of noise coupling between signal nets and power/ground planes at resonant frequencies, including the impact of signal return path discontinuity were studied. Resonance suppression schemes including decoupling

capacitors and ground via placement were investigated [35]. The noise coupling between signal through-vias of silicon and glass interposers were compared by both frequency and time domain simulations [26]. The effects of simultaneous switching noise and signal discontinuity in silicon and glass interposers using M-FDM methods were also compared [62, 63]. The power/signal integrity of PDN with TSVs in lossy silicon interposers and through-glass vias (TGVs) in low loss glass interposers was investigated with a large number of signal I/Os. SSN was identified as a major challenge in glass interposer PDN design [63]. Further, the power delivery design of glass interposers is more challenging than silicon, where the conductivity of Si (10-20 S/m) reduces the resonance magnitude.

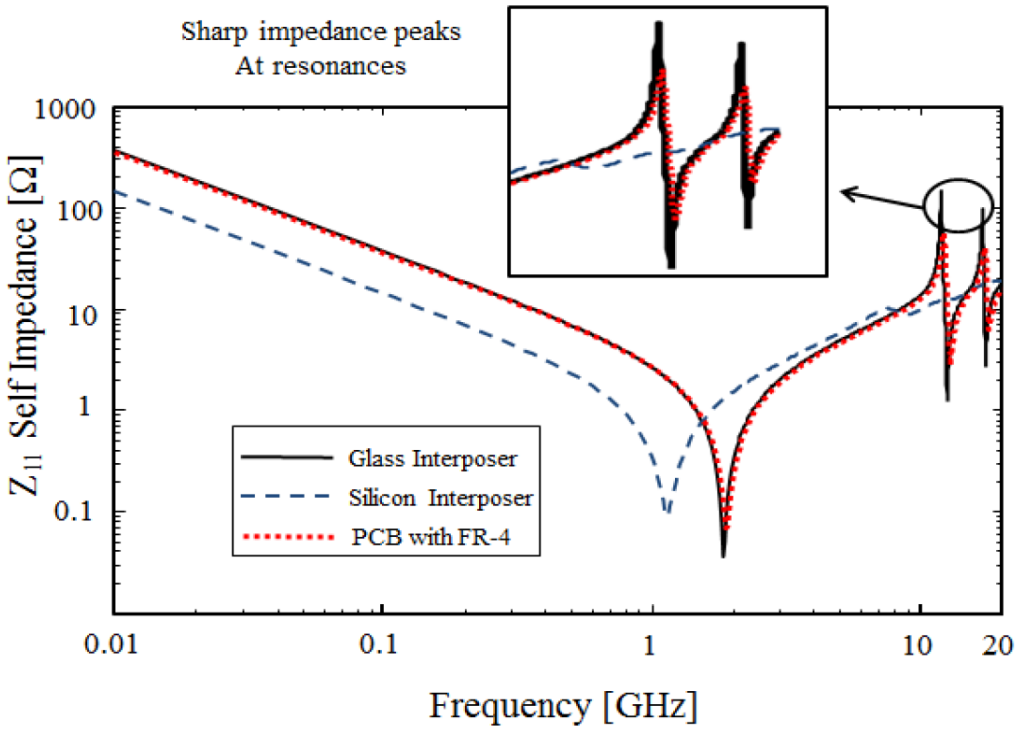


Figure 20: P/G impedance comparison between Glass, Si and Organic packages from [64]

2.3 PDN DESIGN ANALYSIS AND RESONANCE SUPPRESSION TECHNIQUES

The design of power distribution networks in 3D packages presents several well-established challenges [65]. There is a requirement to achieve target impedance over a broad range of frequencies as the standard approach to PDN design in order to avoid supply voltage fluctuations. However, the trend towards supply voltage reduction imposes additional design challenges [66], arising from parasitic inductances and the presence of discontinuities. The presence of split planes and apertures from fragmented high I/O routing was also established to create return path discontinuities (RPD) [67]. Published work on the effects from BGA placement and resonance suppression techniques on PDN inductance are reviewed in this sub-section.

A) BGA placement:

Parametric variations of the PDN characteristics due to the change in (a) number of P/G BGAs and (b) PWB trace length were studied. Multiple PCB design configurations were fabricated and investigated for practical PDN bottlenecks [68]. Reducing the number of P/G BGA pairs from 250 to 50 increased the PDN inductance from 2.8pH to 6.81pH (~4pH). Based on these tabulated findings, it was observed that the mid to high frequency target impedance values may have the most impact from BGA depopulation with the 3D interposer configuration. Further, the BGA location was found to have 5-15% impact on PDN inductance and resistance [69]. The parasitic effects from different power/ground balls positions on PWB were also investigated [70]. To enhance power integrity, the best arrangement of power/ground balls location for both power and ground balls was in the vicinity of the VRM for reducing the length of the current path.

Segmentation methods were used to model impedance changes from board-level placement variations [71]. In addition, RLGC parameters were extracted for different PCB trace lengths. The power path parameters were used to study the SSN performance variations in FPGA applications [72].

B) **Resonance Suppression Techniques:**

The PDN resonance phenomenon has been researched extensively for the past few decades. The approaches to suppress power-ground resonances in glass interposers can be classified into (a) Decoupling techniques and (b) Isolation techniques (EBG, Impedance and termination techniques). A comprehensive overview of these design schemes was presented [74]. This sub-section presents literature on decoupling techniques relevant to 3D-integration.

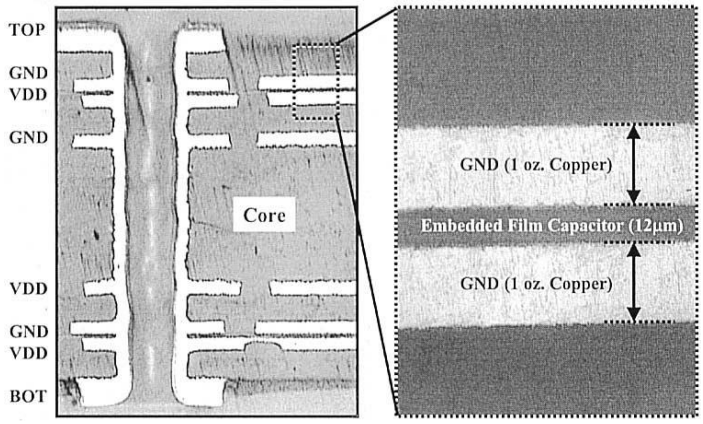


Figure 21: Eight ML stackup to suppress high frequency resonances from [73]

1. Decoupling Capacitors:

The use of hierarchical decoupling capacitors to keep the PDN at low impedance and to provide the necessary transient currents is well established. However, SMT capacitors fail to provide decoupling at higher frequencies due to their high parasitic inductance. On-chip decoupling capacitors occupy valuable real estate, giving rise to the need for

effective decoupling schemes in interposers and packages. Novel decoupling capacitor stacked chips (DCSC) based on additional decoupling capacitor tiers connected with through-silicon-vias (TSVs) have been proposed. This scheme provides several tens of μFs with low ESL (20-50pH) values due to short interconnections from 3D integration [75]. Decoupling capacitors were be integrated as thin-film components or thin integrated passive devices (IPDs) on glass and silicon interposers. Such an approach provided high capacitance close to both dies on a 3D interposer, and can be compatible with high temperature sputtering process [76, 77]. Coaxial through-package-vias (TPVs) with high dielectric constant liners can be used as an effective method to deliver clean power within a 3D glass package. A solution-derived conformal coating process was demonstrated on TPV structures using a vacuum infiltration process [78]. These studies were extended in this dissertation to develop anodized tantalum oxide coaxial decoupling P/G vias for improved power delivery.

2. P/G planes, Substrate and Vias:

The power is distributed to on-chip PDN through one or more power/ground planes on the PCB and the interposer package. These conductive planes form the basis of the system PDN. The effect of dielectric thickness, dielectric constant, and parallel connection of power-ground plane pairs was discussed [79]. Through their inherent skin losses, conductive planes around sufficiently thin dielectric layers similar to glass interposers were found to provide good suppression of plane resonances [80]. Embedded thin film capacitor planes were employed to suppress inductive impedance and SSN till 3GHz [73]. Eight-layer test PCBs were fabricated and power/ground inductive impedance was reduced from 270 pH to 106 pH by using an embedded film capacitor in

place of 16 discrete decoupling capacitors. The planar capacitance of P/G pairs reduces in the presence of multiple vias. The via distribution effects on the multi-layered power/ground impedance was investigated [81]. The lowest effective inductance was observed with a staggered via distribution on the power/ground planes of the packages**.** These substrate effects are studied for the first time in this research in the context of ultra-thin 3D glass interposers.

2.4 Chapter Summary

This dissertation goes beyond published literature to create new scientific knowledge in the areas of power delivery design and demonstration of ultra-thin 3-D glass interposers. For the first time, the studies on P/G plane resonances from low-loss organic and glass substrates will be extended to include the effects of cavity interactions in ultra-thin, double-sided glass interposers. In addition to extending the resonance mitigation solutions from literature, two novel suppression methods specific to glass substrates are introduced, A) embedded decoupling capacitors and B) coaxial P/G vias, to provide distributed capacitance (>1 μF) within the glass PDN. The coaxial P/G vias were further investigated with high-K liners, extending the existing studies on conformal coating of anodized tantalum oxide using glass substrates. These resonance suppression methods were also compared to various solutions based on the substrate stack-up and die configurations, and will be presented in the subsequent chapters.

CHAPTER 3

ELECTRICAL MODELING AND INVESTIGATION OF POWER DELIVERY NETWORKS IN 3-D GLASS INTERPOSERS

This chapter presents the fundamental research in the electrical modeling and simulation of PDN in 3-D glass interposers, to quantify the increase in PDN inductance due to resonances. A simplified power delivery approach using power and ground planes in 30µm ultra-thin, glass substrates was proposed and analyzed to mitigate the high PDN inductance. The fundamental resonance mechanisms were studied from first principles in 3-D glass interposer packages, and compared to 2D glass packages having fully-populated ball grid array (BGA) interconnections. Based on these results, the 3-D PDN self-impedance was evaluated up to 20 GHz, using on-chip, package and PWB full-wave EM models. Following this analysis, the final section discusses the impact of PDN resonances on signal delivery due to signal-to-power coupling. The objective of these investigations was to develop design solutions to address the PDN challenges in 3-D glass interposers, which are presented in the subsequent chapters.

3.1 Modeling and Investigation of Power Delivery Network Resonances

The objective of a power distribution network (PDN) is to provide a clean and constant voltage source to ICs while accommodating current variations arising from circuit switching. Hence, it is critical to provide the lowest impedance power delivery path from the PWB to the device. However, there are fundamental challenges in PDN design in 3-D glass packages, due to the presence of inductive elements, from the printed

circuit board, package and trace inductances, and solder bumps. The resulting P/G resonances can be evaluated based on their self-impedance (Z11) profile.

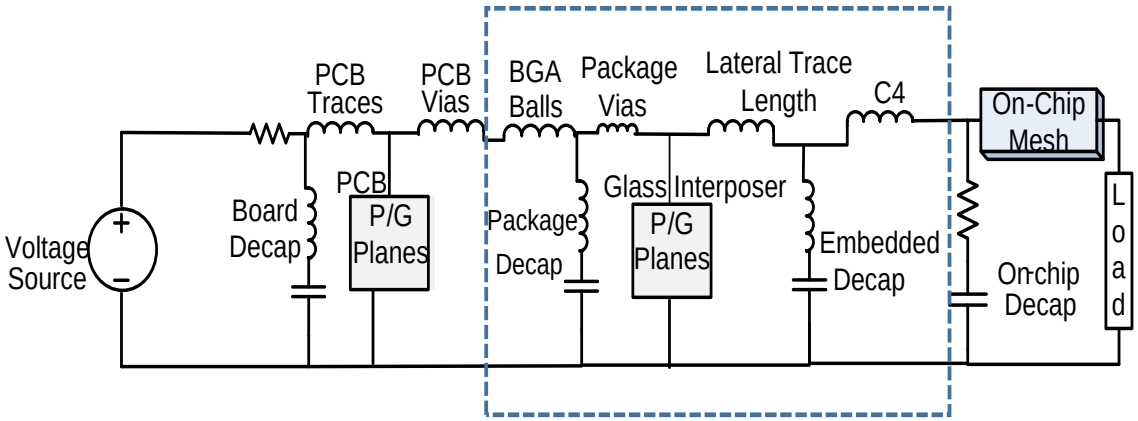


Figure 22 : Power delivery schematic of 3-D glass interposers

The PDN schematic of 3-D glass interposer packages is illustrated in Figure 22. The basic block diagram of a 3-D glass interposer power delivery network can be divided into three parts: (i) Package P/G planes with lateral traces, (ii) TPVs, and (iii) decoupling elements. Based on this model, this section describes the electromagnetic(EM) modeling of the self-impedance (Z11) profile of double-sided 3-D glass interposer power delivery network (3-D PDN) and analyzes the P/G resonances as the critical step towards clean power delivery. In this study, the term "2-D PDN" refers to a single-sided glass interposer PDN with a fully populated BGA array, and "3-D PDN" refers to a double-sided glass interposer PDN with a centrally depopulated BGA array. The inductances of the different entities of this proposed system were estimated through 3D-EM simulations and analytical models [82, 83]. Although the individual parasitics of vias and interconnects were high, their equivalent resistance dropped to very low values due to the

large number of structures connected in parallel. Table 3 shows the inductances along with the total PDN parasitic values. The trace inductances of power or ground planes were observed to far exceed the equivalent inductance of the TPVs and thus contribute significantly to the impedance characteristics of the package.

Table 3: Inductance values of various PDN interconnects

Package Interconnect	Estimated loop inductance	Estimated no. of parallel pairs	Equivalent Inductance
BGA solder @ 500µm pitch	152.9 pH	300-700 pairs	0.5pH – 0.21pH
Micro-C4 @ 500µm pitch	14.3 pH	2000	7.15fH
TPV/pair @ 60µm pitch	49pH	2000	0.025pH
Plane Trace	150 pH	-	150 pH

a) Study of Power and ground plane resonances in glass interposers

P/G planes form the fundamental building block of the 3-D glass-interposer PDN. Hence, this section provides a detailed comparison of P/G resonances between glass, silicon and organic interposers. The power-ground planes were modelled as parallel plate waveguides to support different resonance modes between the conducting surfaces. These resonance modes correspond to frequencies that can support a standing wave in the cavity. A simple expression from literature [82] that predicts the resonant modes in a parallel plate waveguide whose lateral dimensions far exceed its height can be written as:

$$f_r = \frac{1}{2\pi\sqrt{\mu\varepsilon eff}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \quad (2)$$

where: f_r = resonant frequency
a,b = length and width of the structure
m,n = mode numbers; =0,1,2,…
$\mu, \varepsilon eff$ = Permeability and effective permittivity of dielectric

This expression indicates that the resonances shift to lower frequencies with increasing dielectric constant. The electrical properties of materials used in the simulation and fabrication of the glass interposer packages are tabulated in Table 4. In addition to silicon, glass and organic interposers, an on-chip PDN was also included to provide a baseline for the comparison. The double-sided 3D interposer packages used in this study have the P/G planes located in the inner two-layers on either side. Copper planes having a thickness of 10 µm were simulated using a full-wave EM solver (Ansys-HFSS™) with an interposer size of 10mm x 10mm. ZEONIF™ -ZS material was used as both the lamination layer and build-up dielectric layer. This dielectric was used as the primary polymer in this research study. The simulated self-impedance profile till 20GHz observed at the center of all the interposers was plotted as presented in Figure 23. The 30 µm glass interposer with P/G planes had the lowest impedance due to added capacitance arising from the ultra-thin core. However, it still exhibited high magnitude resonances at GHz frequencies when compared to the silicon interposer, due to its low dielectric loss and high quality factor. There are multiple dielectric materials between the planes on the core, so the effective permittivity of the P/G plane cavity was computed as shown in the equation (3) based on the method presented in [64].

$$\varepsilon_{eff} = \frac{h_{glass+2\times polymer}}{\frac{h_{glass}}{\varepsilon_{glass}} + \frac{h_{polymer}}{\varepsilon_{polymer}} \times 2} \quad (3)$$

Since the microwave modes are determined by the properties of the P/G cavity, it was possible to select polymer materials having the required thickness and electrical properties to achieve the desired resonance frequencies.

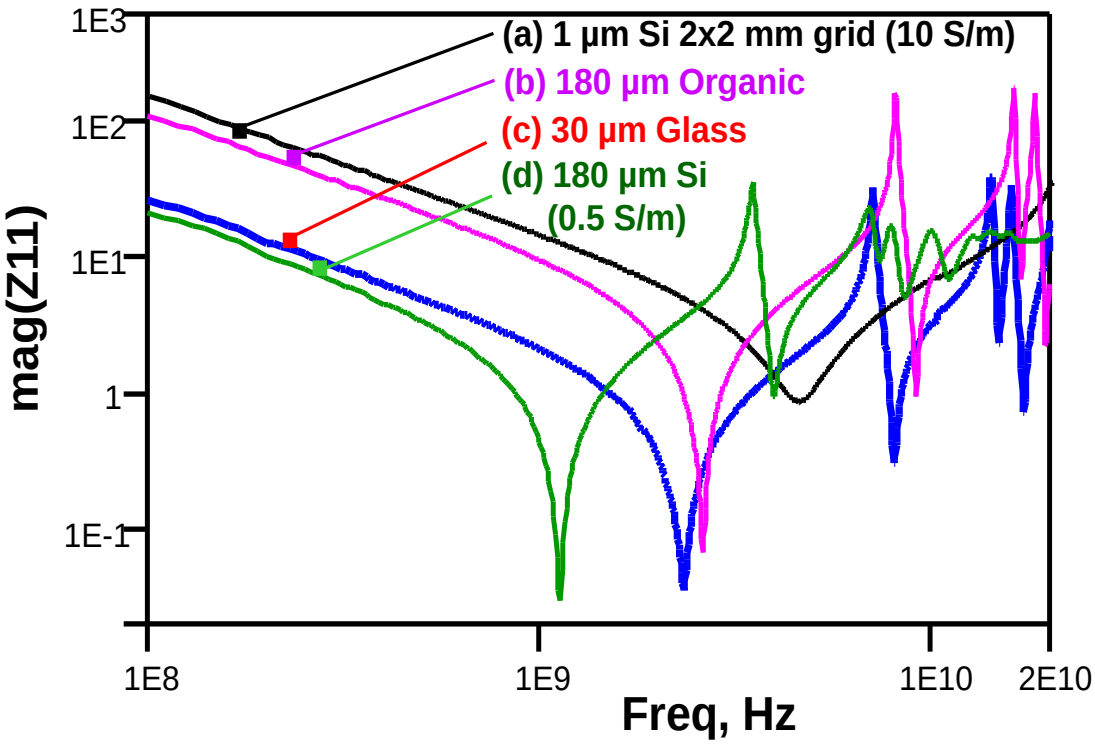


Figure 23: Comparison of P/G resonances for different interposer package materials

Table 4 : Properties of interposer package materials for simulation and fabrication

Material	Dielectric Constant (ε_r)	Loss tangent (tan δ)	Thickness available (µm)
Borosilicate Glass	5.5	0.006	30 µm; 100 µm
ZEONIF™ - ZS polymer (Polymer Dielectric)	3.1	0.005	8 µm; 17.5 µm
Low-resistivity Silicon	11.9	Cond: 0.5 S/m	180 µm
High Resistivity Silicon	11.9	Cond: 10 S/m	50 µm

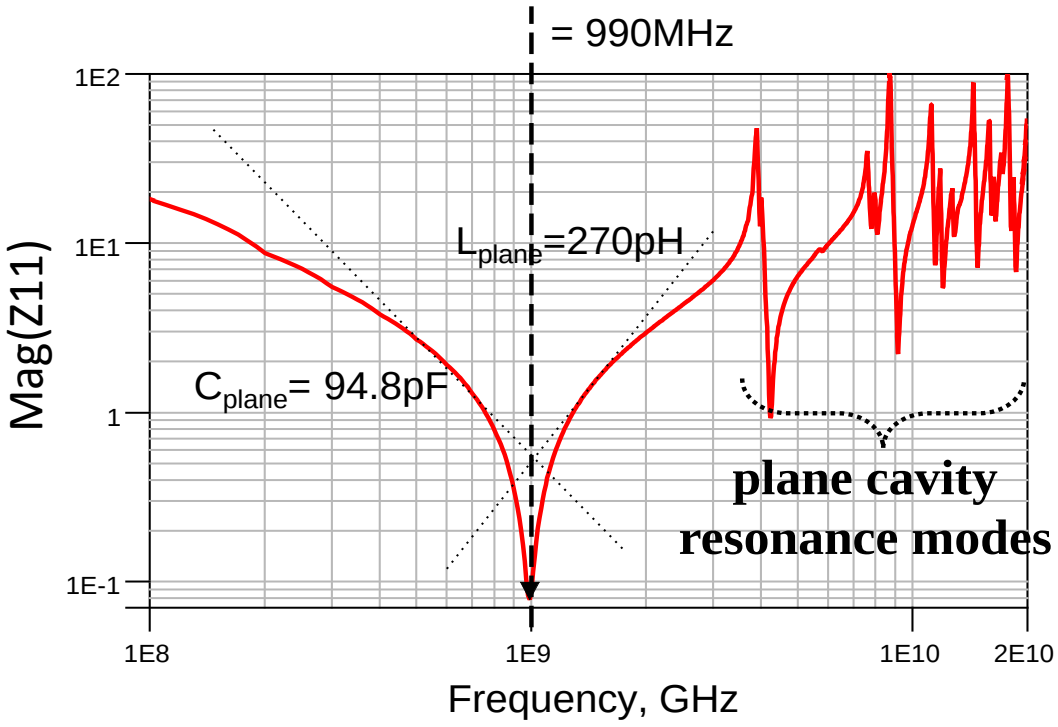


Figure 24: P/G resonances in 100-µm thick glass, 17mm x17mm interposer

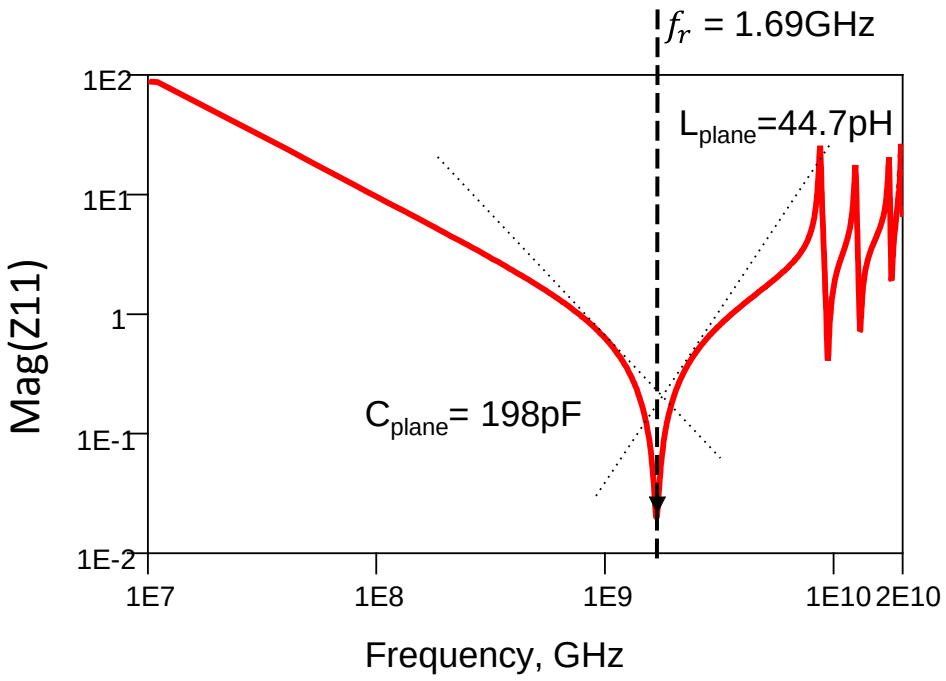


Figure 25: P/G Resonances in 30-µm glass 10mmx10mm interposer

The capacitances and the plane inductances were extracted from the values of the first series resonant frequencies. The self-impedance (Z11) at the center of the 17mm x 17mm P/G planes across the 100µm thick glass was plotted as shown in Figure 24. The values for the 10mm x 10mm 30µm thick glass interposer are shown in Figure 25. The improved suppression in the case of the 30um glass occurs due to the thickness reduction between the power and ground layers, when compared to the 100µm-thick glass. Changing the interposer dimensions alters the resonant modes due to cavity variations. The L and C values for 17mm x 17mm interposer in 100 µm glass with 17.5 µm polymer dielectric was extracted from the plot in Figure 24. The plane inductance increased due to a combination of larger cavity length and greater distance between the planes. The observed cavity modes are listed in Figure 26 and Table 5.

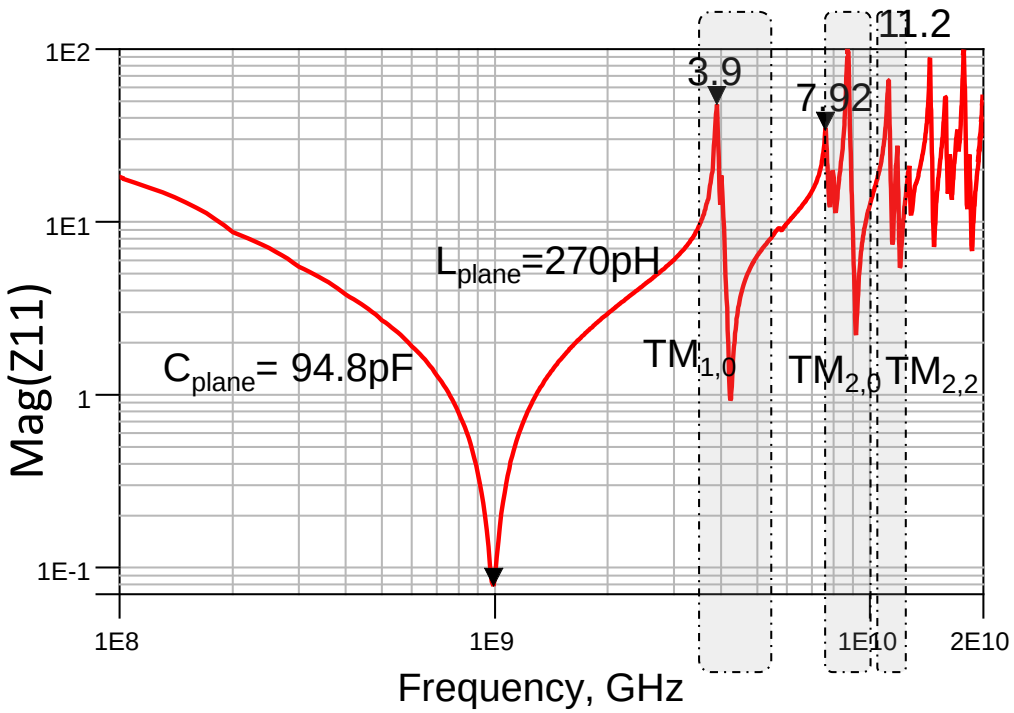


Figure 26: Analysis of resonance modes in 100-µm glass

Table 5: Resonance modes observed in 17x17mm glass power-ground planes

Mode Number		Frequency of impact (GHz)
m	n	
1	0	4.01
1	1	5.51
2	0	7.8
2	1	8.81
2	2	11.05
3	0	11.8

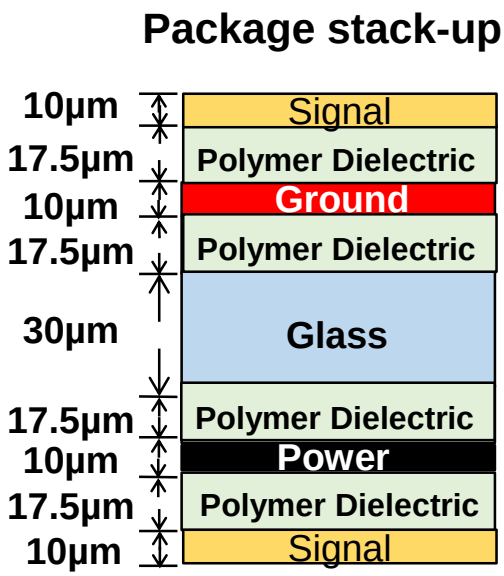
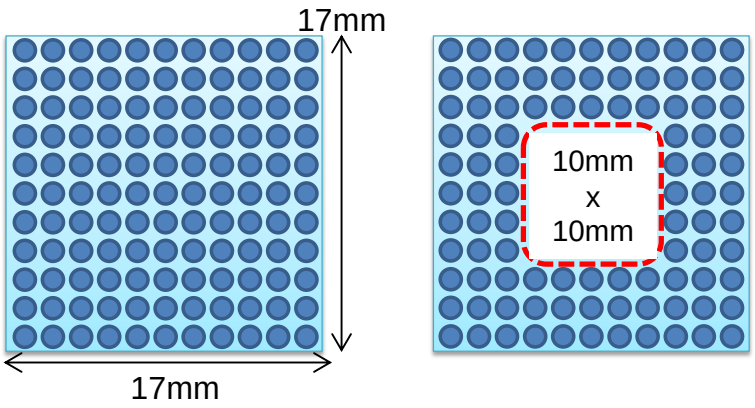


Figure 27: 3-D glass interposer package stack-up

b) Comparison of 2-D and 3-D glass interposer PDN resonances

The PDN self-impedance of glass packages having fully-populated ball grid array ("2D-PDN") was compared to that of glass packages having centrally-depopulated BGA's ("3D-PDN"). This BGA variation due to the placement of the bottom die in 3D interposer packages is illustrated in Figure 28

Figure 28. The magnitude of total self-impedance (Z11) was generated by interconnecting separate multi-port P/G 3-D EM models with their corresponding parasitic interconnections. A cross-section schematic of the stack-up of the glass interposer package used for full wave simulation of the multi-port glass interposer P/G planes is shown in Figure 27. Due to the very large number of P/G nets involved in such a full system PDN analysis, a simplified architecture was considered in this study with the interposer PDN formulated using grouped BGA and C4 locations. The port locations and setup used for this simulation are illustrated in Figure 30.



No. of P/G BGA pairs	**700**	**300**

Figure 28: Bottom View of BGA Solder Ball comparison between 2-D and 3-D PDN

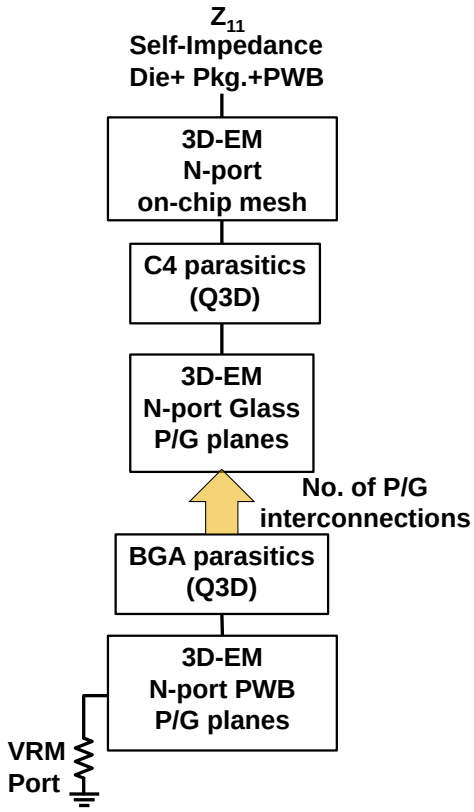


Figure 29: Self-impedance simulation methodology for 3-D glass interposers

The PDN simulations for different PDN configurations were performed in Agilent ADS™ after combining the multi-port 3D-EM models with lumped parasitic values. Parasitic inductances were added to the port locations based on the total number of parallel BGA connections for each configuration represented by M (700 pairs) and N (300pairs). The multi-port simulation methodology is illustrated in Figure 29. The multi-port glass package model was then grounded at port locations based on the BGA configuration.

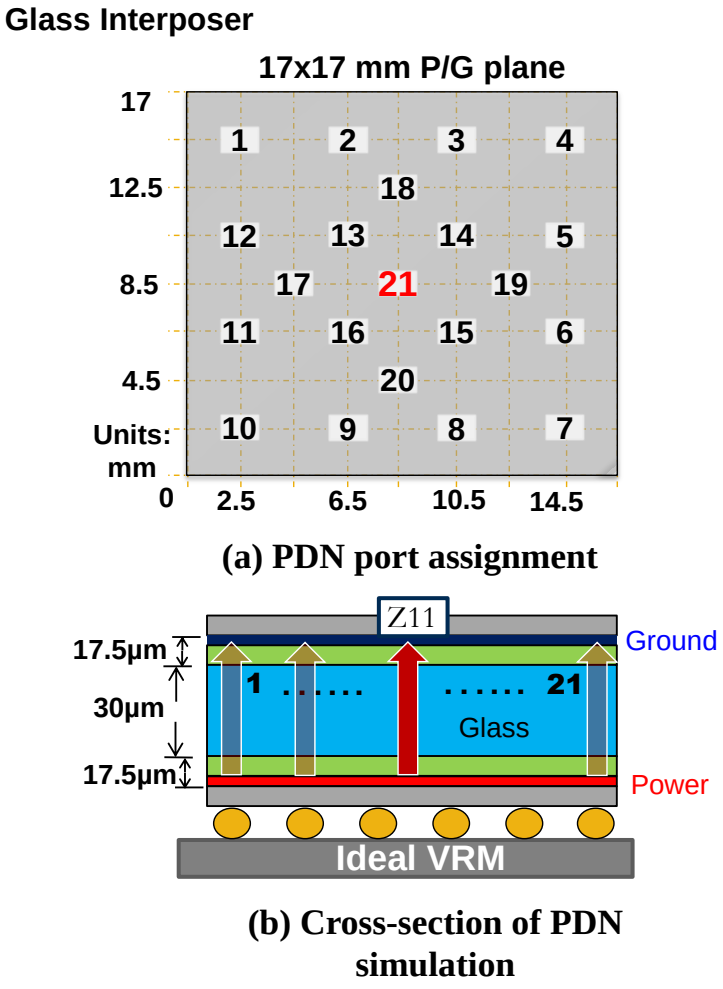


Figure 30: Port mapping and assignment

The comparison of the PDN self-impedance between the glass interposer P/G plane and variations from the BGA connections is summarized in Figure 31. The PDN resonances and anti-resonance nulls were interchanged due to the addition of second-level interconnections to the voltage source. Therefore, this result was used to determine the impedance of the overall glass interposer PDN based on BGA variations. The simulation was performed with the printed wiring board (PWB) connections to the voltage source path represented by ideal ground with reduced number of P/G BGAs ('N') due to the placement of the die as shown in the schematic in Figure 32.

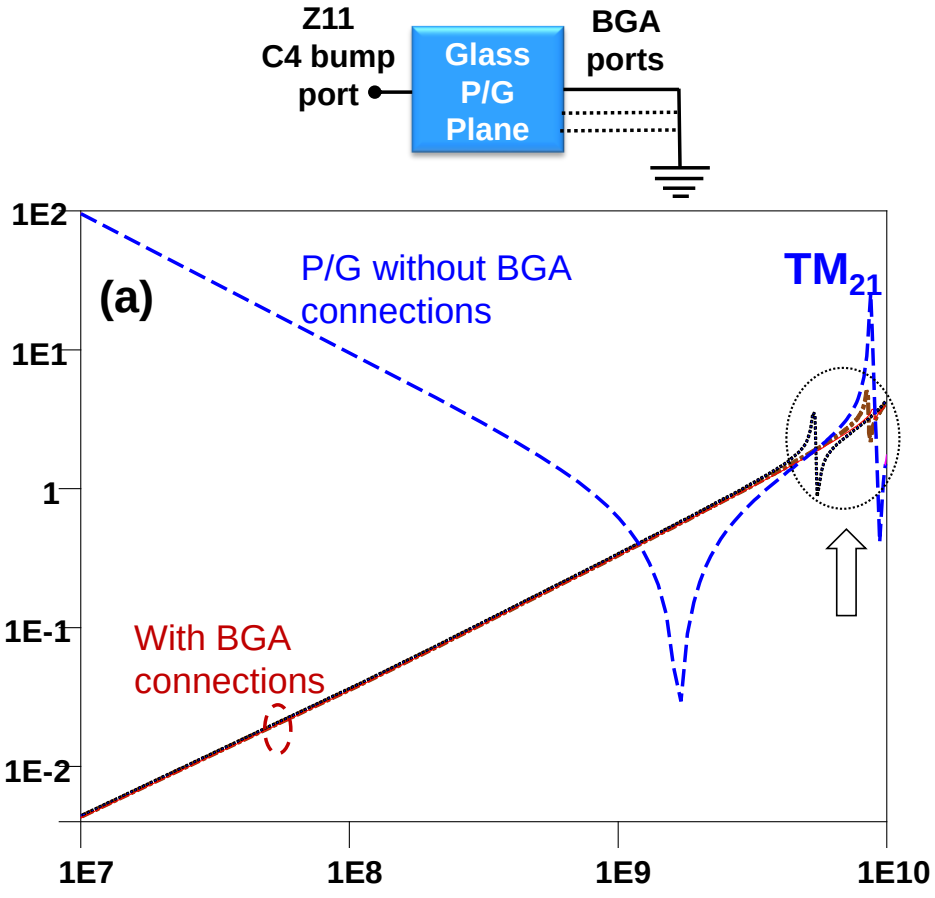


Figure 31: PDN simulation methodology with BGA and P/G planes

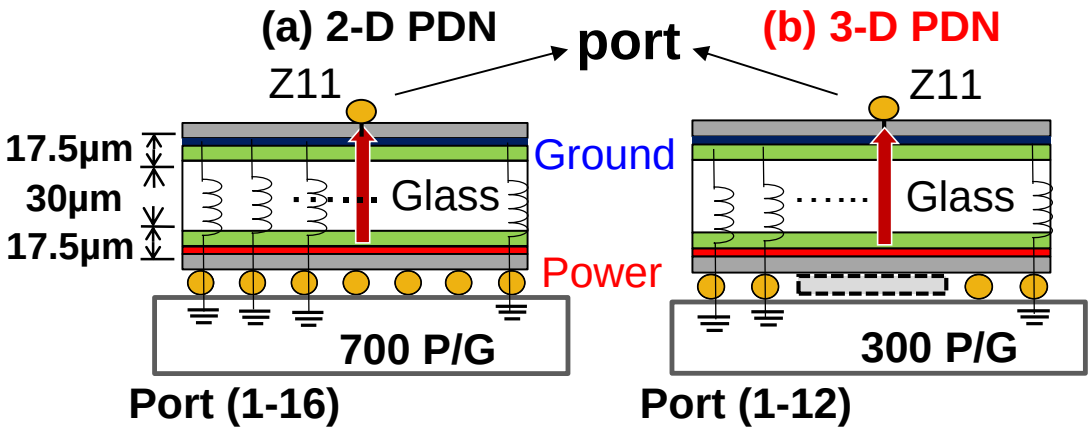


Figure 32: Port setup for 2-D and 3-D PDN simulation

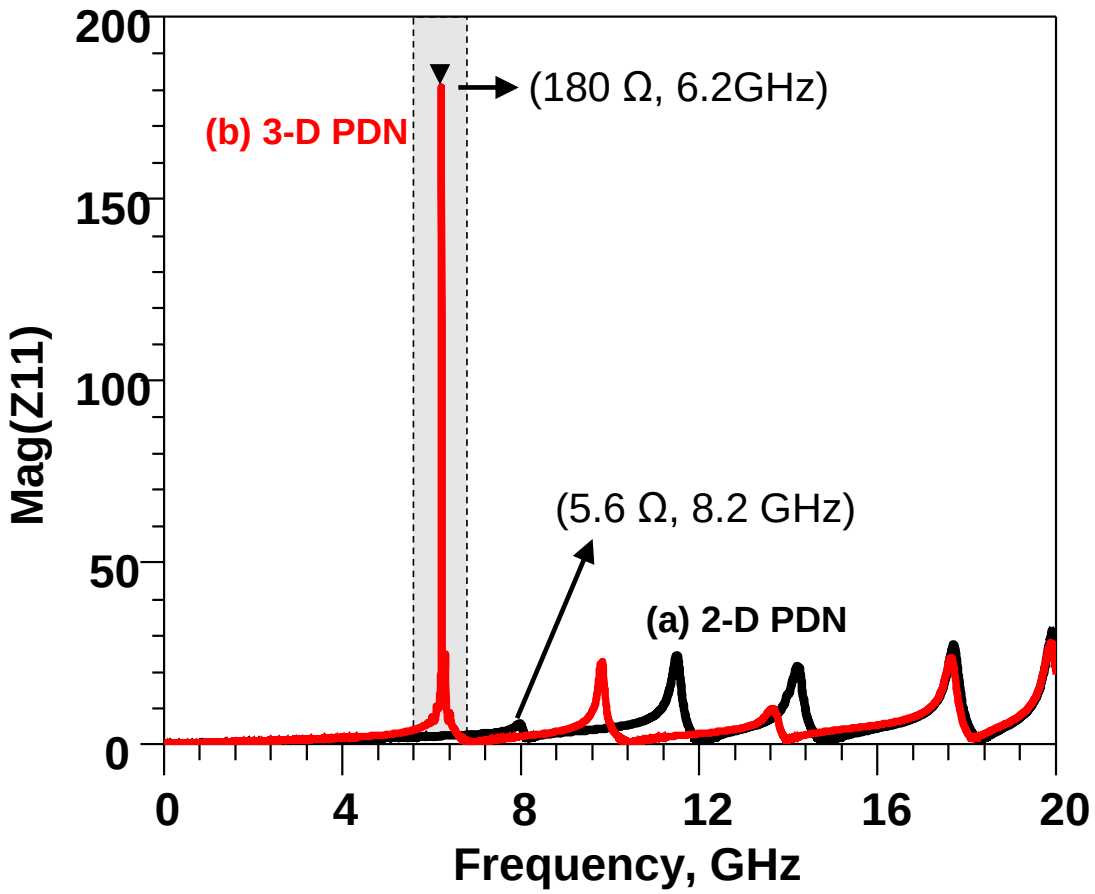
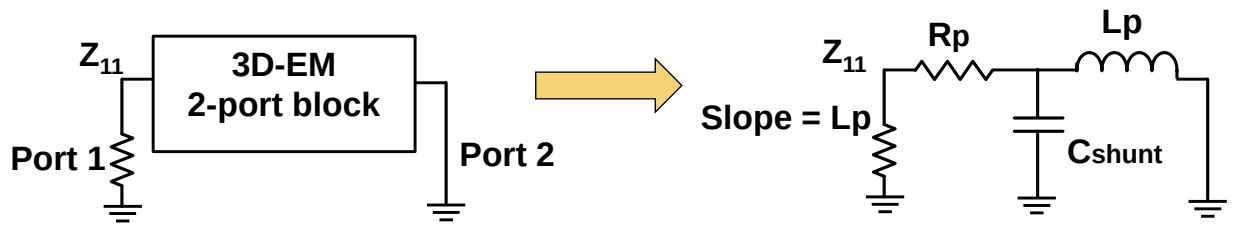
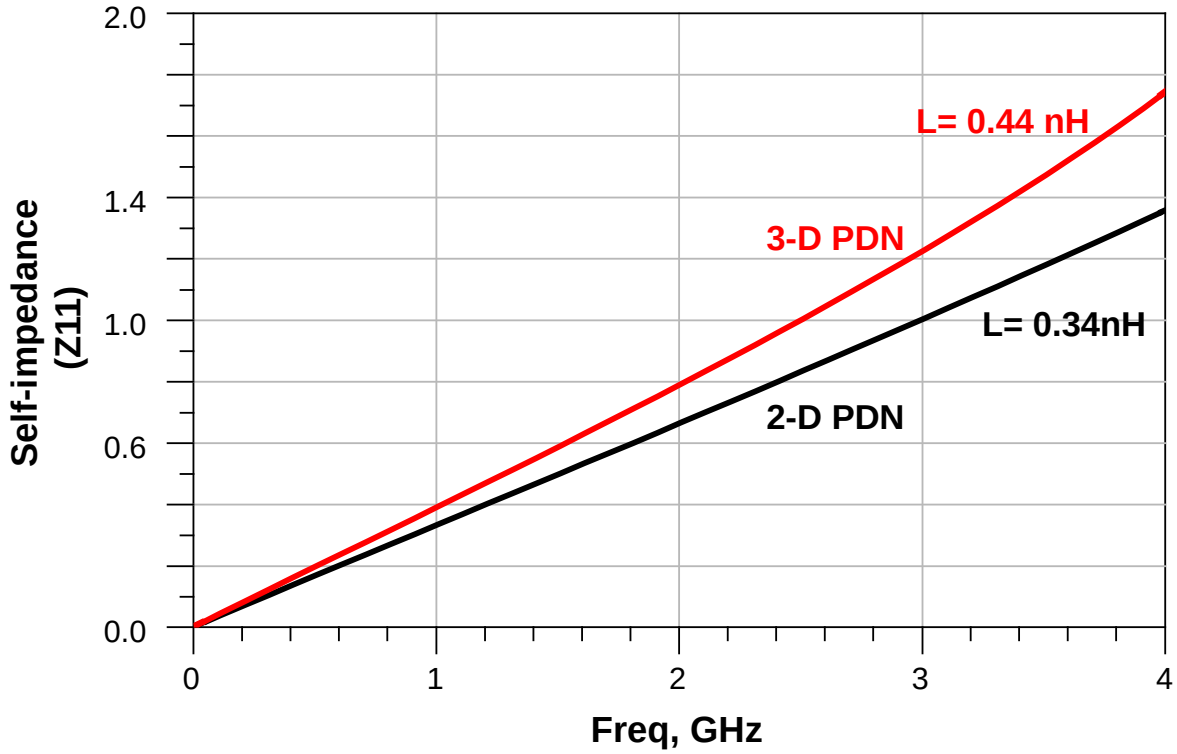


Figure 33: Comparison of 2-D Vs. 3-D glass interposer PDN without on-chip and PWB PDN



(a)



(b)

Figure 34: (a) Extraction and (b) Comparison of 2-D Vs. 3-D glass interposer PDN inductance

The simulated comparison between the 2D and 3D glass package configurations is shown in Figure 33. The interaction between the P/G plane cavity and the lateral traces in the case of the 3-D PDN generated much larger anti-resonance peaks: 180 Ω for 3-D PDN vs. 5.6 Ω for 2-D PDN. Additional loop inductance was also observed in the 3-D case, due to the reduction in the total number of BGAs. The differences between the

higher order mode resonances were negligible at very high frequencies beyond 15 GHz. The first anti-resonance frequency in the 3-D PDN was shifted to a lower frequency (6.2 GHz). This caused the overall core-PDN bandwidth to be reduced by 2 GHz at the interposer due to the double-sided die attach structure. Hence, meticulous suppression of PDN resonances and appropriate signal routing is necessary to suppress SSN in 3-D glass interposer packages. However, the parasitic inductances of the lateral traces were smaller than the P/G planar capacitance, leading to high-impedance peaks only at frequencies beyond 6 GHz.

Based on this study, the parasitic inductance of the total interposer package was extracted as shown in Figure 34b. The package port connecting to the BGA locations were grounded in order to shunt the package capacitance. Therefore, as seen from the proposed circuit schematic in Figure 34a, the package inductance was determined using the slope of the impedance curve computed at port in the center of the interposer. At frequencies below 5 GHz, the inductance values for both 2-D and 3-D PDN based on two different BGA configurations were 0.34nH and 0.44nH, respectively. Thus, the additional loop inductance due to the reduction in the total number of BGAs was of the order of tens to hundreds of pH (110pH), which may pose significant challenge in 3-D PDN design requirements.

c) PDN Modeling of 3-D glass interposer package, PWB and on-chip grid

This section builds on the EM modeling of interposer PDN from the previous section, to evaluate the total self-impedance of 2-D and 3-D PDN including the effects of on-chip P/G grid and PWB P/G planes. The magnitudes of self-impedance (Z11) at the system

level were generated by interconnecting separate multi-port P/G 3-D EM models of on-chip grid, glass interposer, and the PWB planes with their corresponding parasitic interconnections as shown in Figure 35.

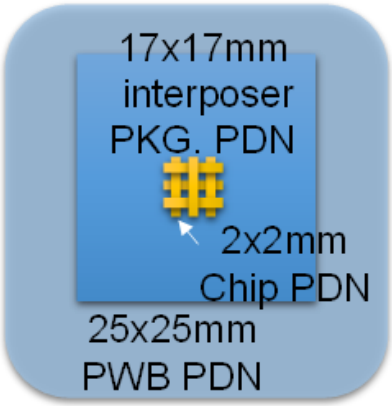


Figure 35: Dimensions of on-chip grid, glass interposer package and PWB P/G planes

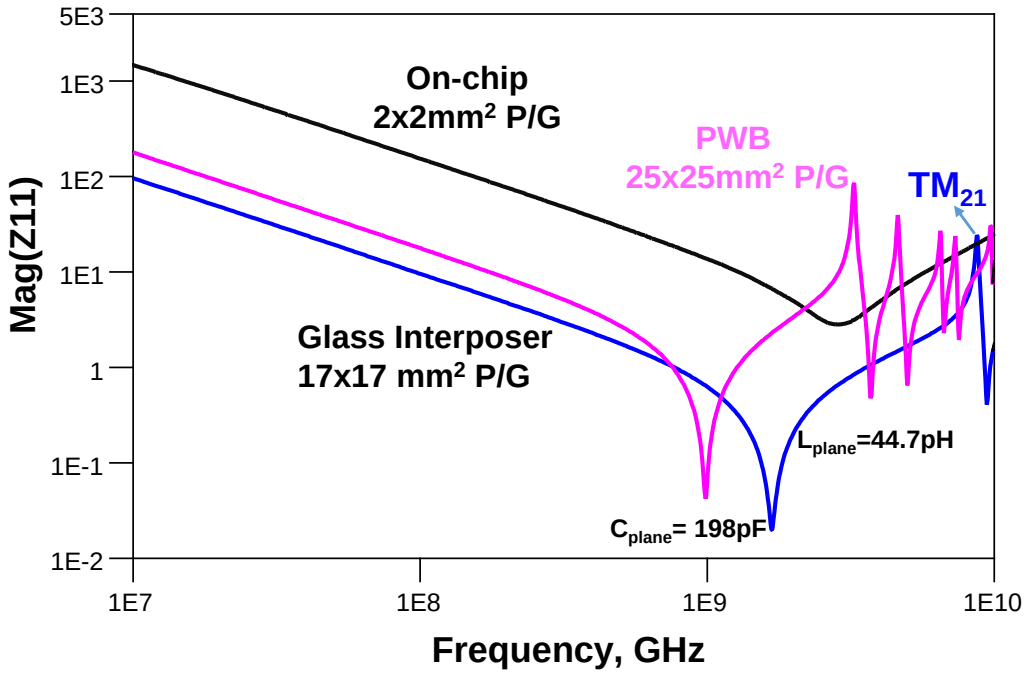


Figure 36: Self-impedance for on-chip grid, glass interposer package and PWB P/G planes

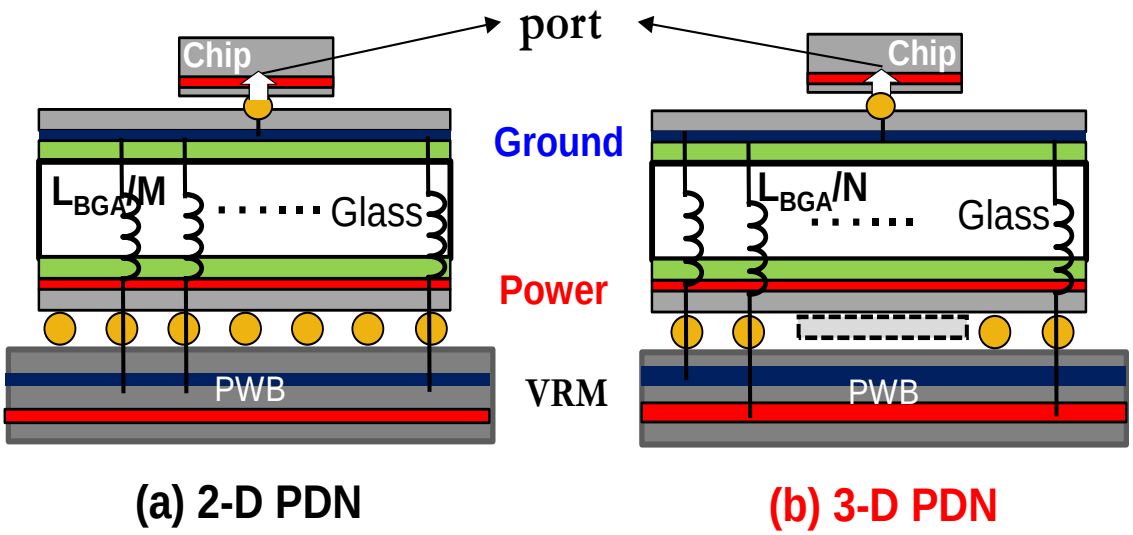


Figure 37 : Self-impedance simulation of system PDN

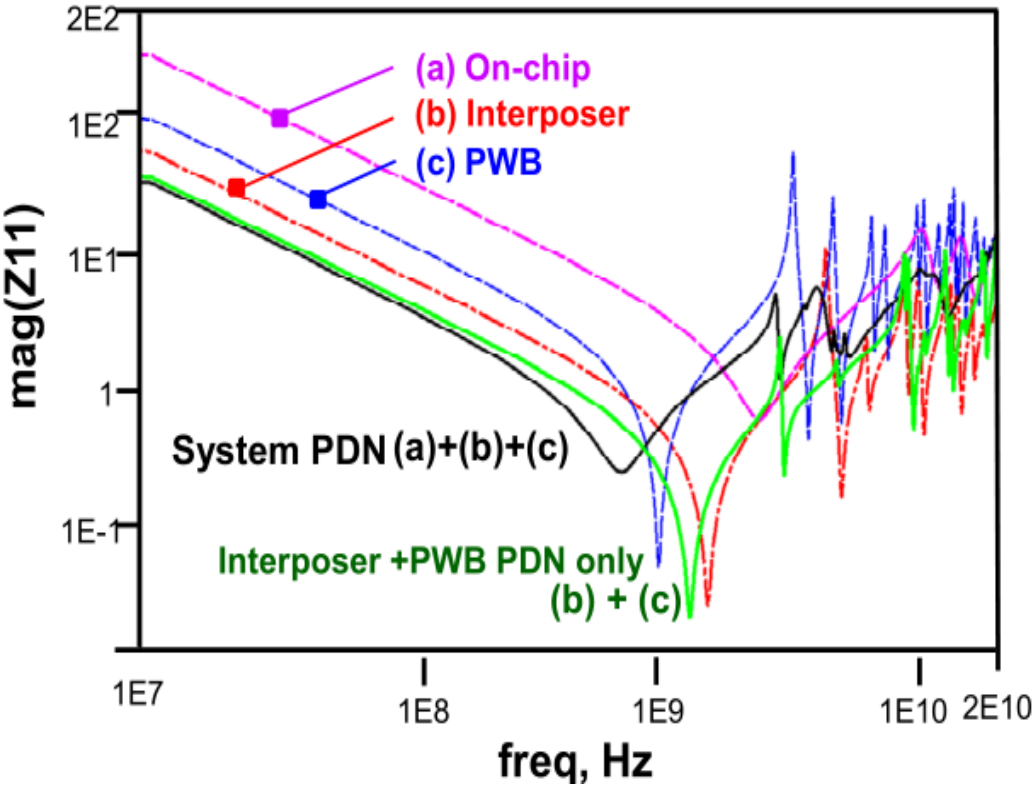


Figure 38: Combination of PDN elements

The simulated self-impedance observed at the center of on-chip grid, glass interposer and PWB P/G planes are plotted in Figure 36. It was observed that the 30 μm thick glass interposer with P/G planes had the lowest impedance, when compared to other substrates, due to its thin core and thicker P/G planes with lower resistivity. The effective permittivity of the P/G plane cavity was computed based on the method presented in [64]. In this simulation, the TM_{21} mode for the glass interposer was observed at the center.

d) Investigation of system-level PDN

The self-impedance (Z11) of the overall system as seen from center of the on-chip P/G grid was simulated by combining multi-port 3-D EM models of hierarchical PDN elements from Figure 36. In the simplified package architecture, power and ground TPVs were ignored in the 3D EM model, due to their negligible parasitic inductance. The PDN analysis was performed from the die model through die-to-package interconnections, package P/G planes, BGAs and terminated at the board P/G plane model. The simulation schematics used to perform the overall-PDN analysis are illustrated in Figure 37. The PDN configurations of 2-D and 3-D interposers were estimated based on the variation in the number of package-PWB port connections. The overall PDN at high frequencies was dominated by the on-chip PDN grid due to its high resistivity, as shown in Figure 39. The system PDN was observed to be the sum of its individual P/G elements.

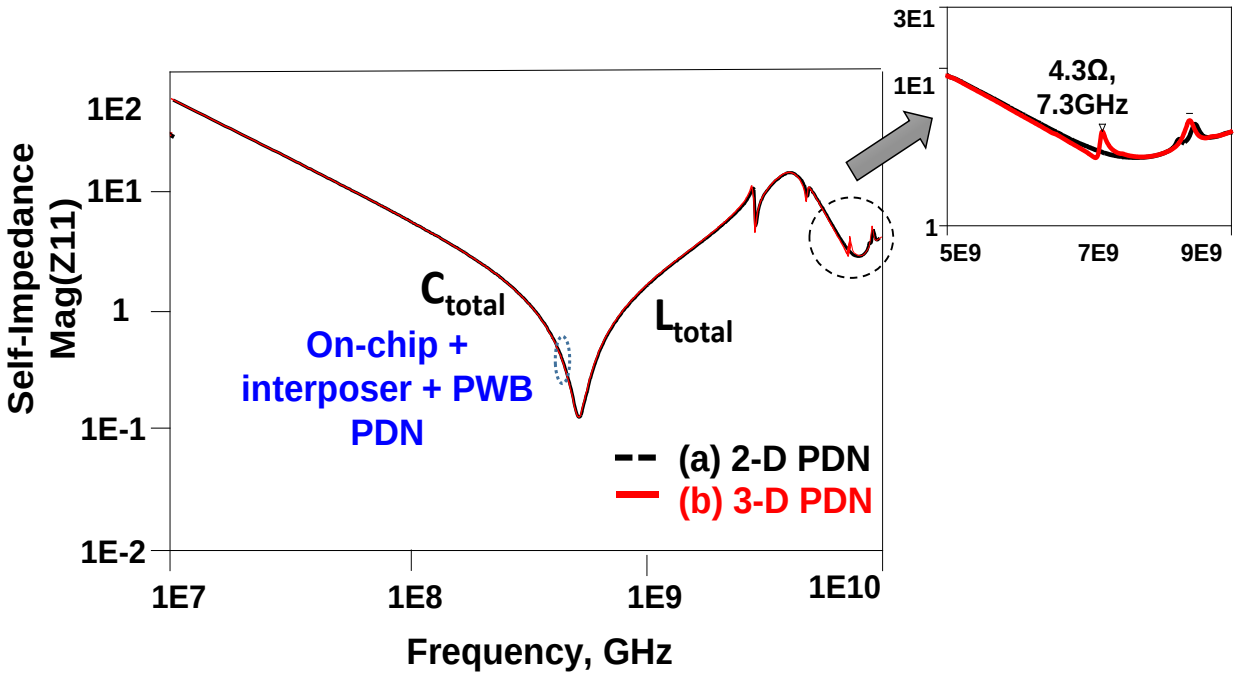


Figure 39: On-chip+Interposer+PWB self-impedance comparison between 2-D Vs. 3-D glass interposer PDN

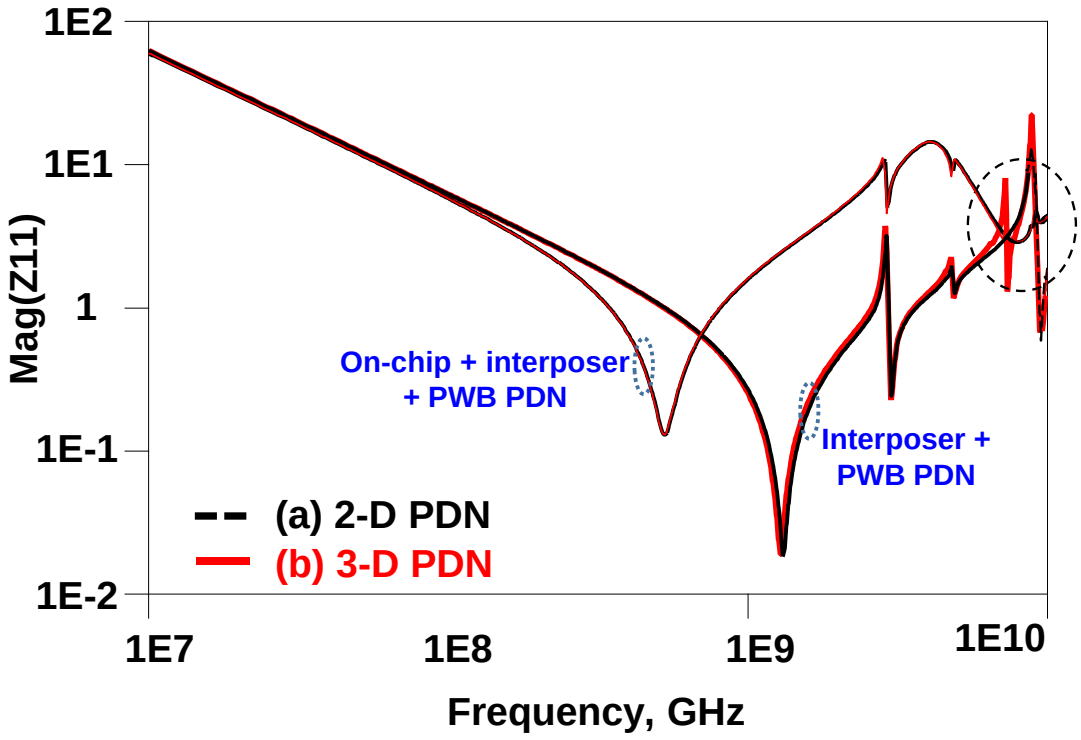


Figure 40: System comparison of 2-D Vs. 3-D PDN

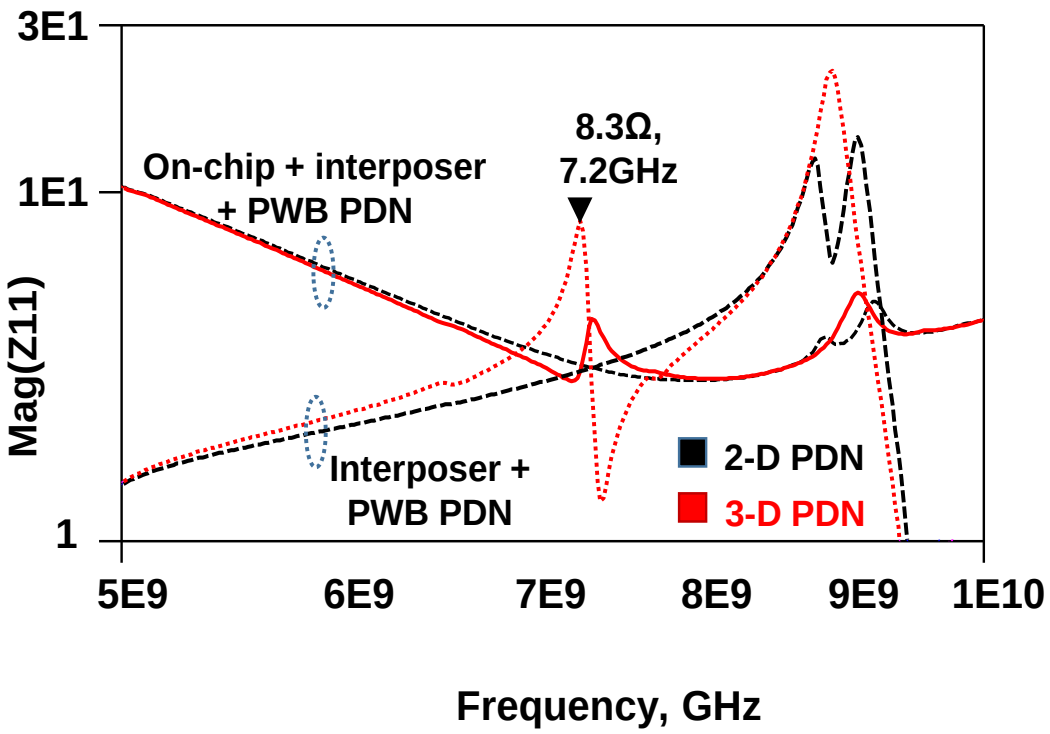


Figure 41: System vs. Interposer+PWB only comparison

The system PDN impedances for 2-D and 3-D interposer packages before and after the addition of on-chip PDN are compared in Figure 40. Resonances were observed for the 3-D configuration near 7.3 GHz, which created high impedance anti-resonant peaks. The resonant peaks in the interposer+PWB correlated directly to the high-impedance peaks observed in the overall-PDN as shown in Figure 41. However, the magnitude of the self-impedance observed at the on-chip location (on-chip+interposer+PWB) was lower by 4Ω when compared to the interposer+PWB. This effect was attributed to the high value of on-chip impedance at frequencies beyond 4 GHz, which dominated the overall PDN profile. Since the transient current demand from the on-chip core-PDN at such frequencies is negligible, this result suggests that the impact of BGA reduction on overall core-PDN system impedance at lower frequencies is

minimal. However, suppression methods are necessary to meet the target impedance guidelines across all frequencies, due to the high-resistivity of the glass substrate.

3.2 Impact of PDN resonances on Signal integrity

The P/G resonances introduced by the 3-D glass interposer package structures described in the previous section create technical challenges for signal integrity by increasing the noise at the power supply pins. Therefore, it is necessary to investigate the impact of resonances on signal integrity to achieve high bandwidth interconnections. This study was performed by simulating the chip-to-PWB signal channels by including the effects of signal-to-power coupling due to resonances. The signal interconnections in 3-D interposers can be classified into (a) Chip-to-Chip Wide-I/O and (b) External Chip-to-PWB I/O, as shown in Figure 42. The presence of the PDN network will have varying impact on each of these signal traces based on their routing length, location, and reference arrangement.

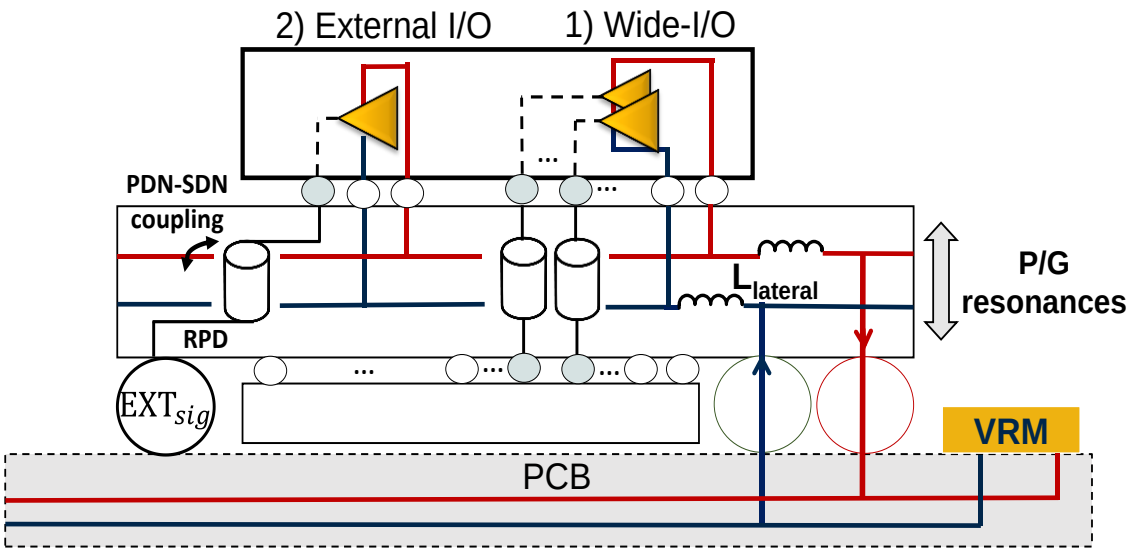


Figure 42: Impact of PDN resonances on signal I/O in 3-D glass interposers

Detailed investigations, comparing the wide-I/O chip-to-chip signal path in the 3-D glass interposer approach with 3D-ICs indicated the ability of the wide-IO through-package-Via interconnects to achieve high bandwidth (>100GB/s) [84]. The coplanar waveguide (CPW) transmission lines consisting of TPVs and RDL traces on 30µm and 180µm glass substrates were designed, fabricated and characterized, demonstrating very low insertion loss (0.06dB/mm) [32]. The 30µm glass interposer also had the lowest loss for all trace lengths with 7% power loss, which is followed closely by 3DICs with TSVs having 11% power loss.

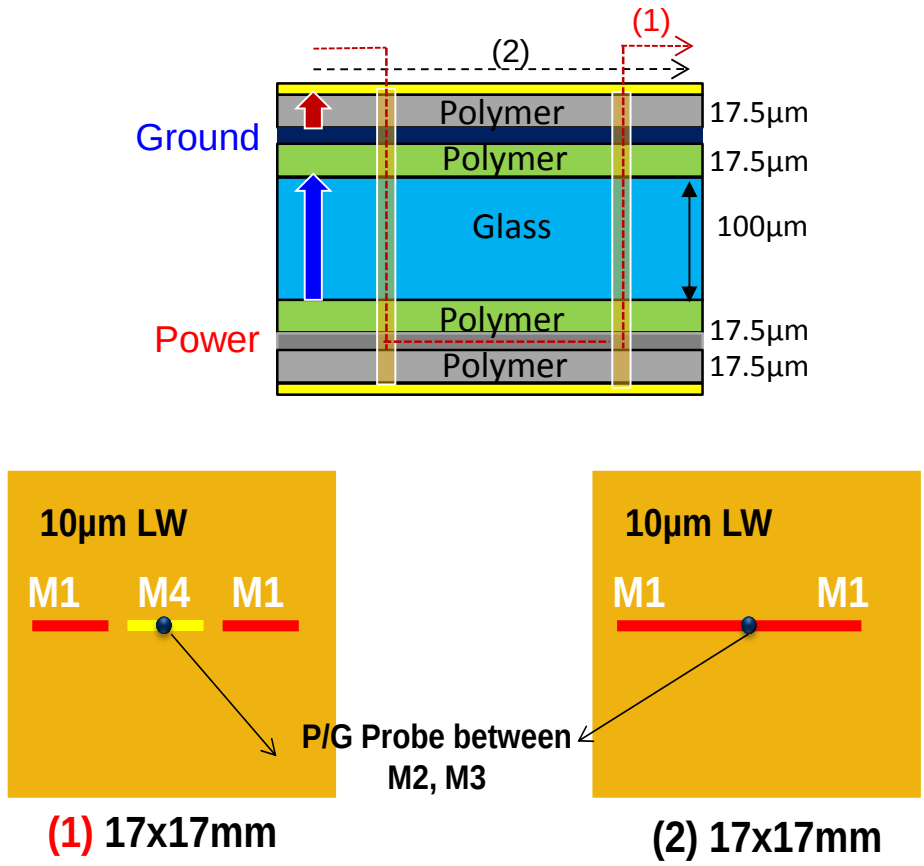


Figure 43: Stack-up materials and Dimensions

This section will focus on the modeling of external I/O signal lines in glass interposers in the presence of return path discontinuities. The signal lines from the chip to the PWB were routed in the presence of discontinuities at power-ground (P/G) resonance frequencies with lateral signal traces near the interposer planes. The RDL wires were modeled as microstrip lines (MSL) on the top and bottom surfaces of the glass interposer using 3-D EM simulations. The cross-section view and model dimensions are described in Figure 43. The glass interposer was designed with 17mm x 17mm power and ground planes located on either side of the 100µm glass core laminated with 17.5um polymer, which served as the dielectric material. The chip-to-PWB signal lines consisted of 5mm line segments with TPV transitions. When the signal was routed through the P/G planes, the return-current flowed on the ground plane while there were referencing discontinuities created at the Through-Package-Via locations.

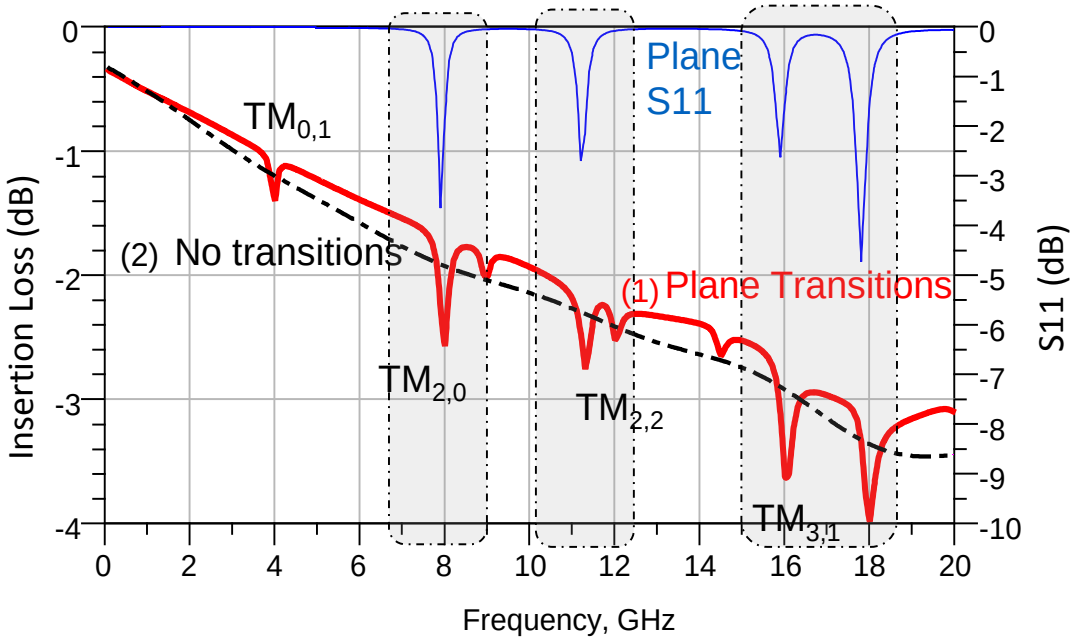


Figure 44: Insertion loss investigation including P/G planes in chip-to-PWB channel

To analyze this discontinuity, routing lines of the same length, with and without TPV transitions were compared, as described in Figure 43 (a). The self-impedance was also simulated at the center of the PDN in order to correlate the insertion loss and plane impedance responses. The simulated insertion loss responses of both scenarios are presented in Figure 44. The glass interposer channel without signal TPVs showed a very uniform insertion loss, that is around -2 dB up to 10GHz. However, the channel with TPV transitions exhibited high magnitude intermittent insertion losses at certain resonance frequencies. The specific mode frequencies (2,0), (2,2) that were observed across the plane pairs correlated well to the insertion loss variations as illustrated in Figure 44.

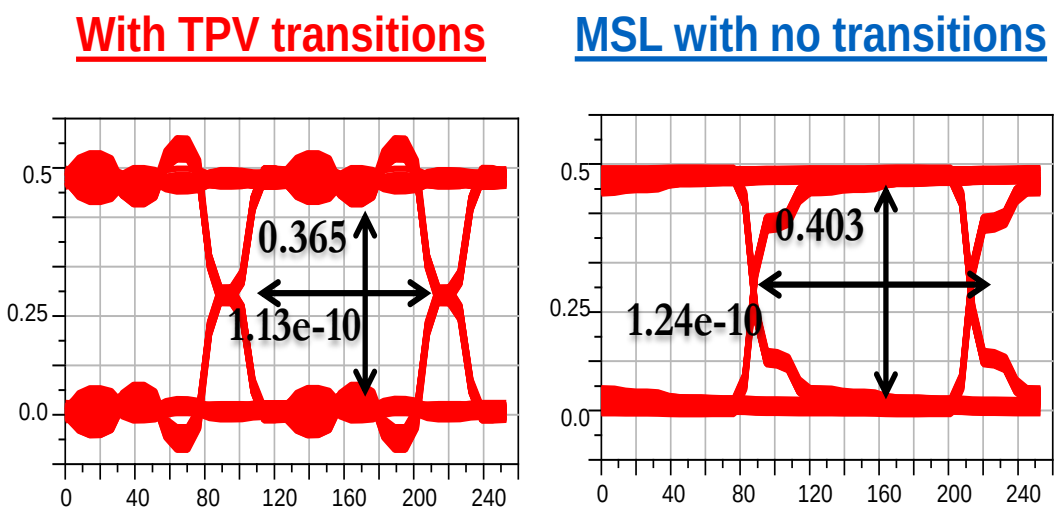


Figure 45: Eye diagram at 8 Gbps

This effect was further analyzed through eye diagrams and noise- coupling simulations. The simulation was carried out in Agilent ADS using a PRBS signal with amplitude of 1V. The simulated model consisted of signal lines, routed through power-ground planes. The multi-port S-parameter block was generated using full-wave EM simulations. The source was placed at port 1 and the eye diagram was simulated at port 2.

The input and output terminations were matched to 50 ohms. An input source was assigned using 0-1V clock with rise and fall time of 10ps. The structure was simulated at 8Gbps corresponding to mode (2,1) and (1,2) resonances. Similar to the insertion loss parameters, the eye diagram was distorted at the resonance frequencies as shown in Figure 45. The peak-to-peak distortion and eye width distortion for the glass with TPV transitions correlated well with the predicted values from previous modeling.

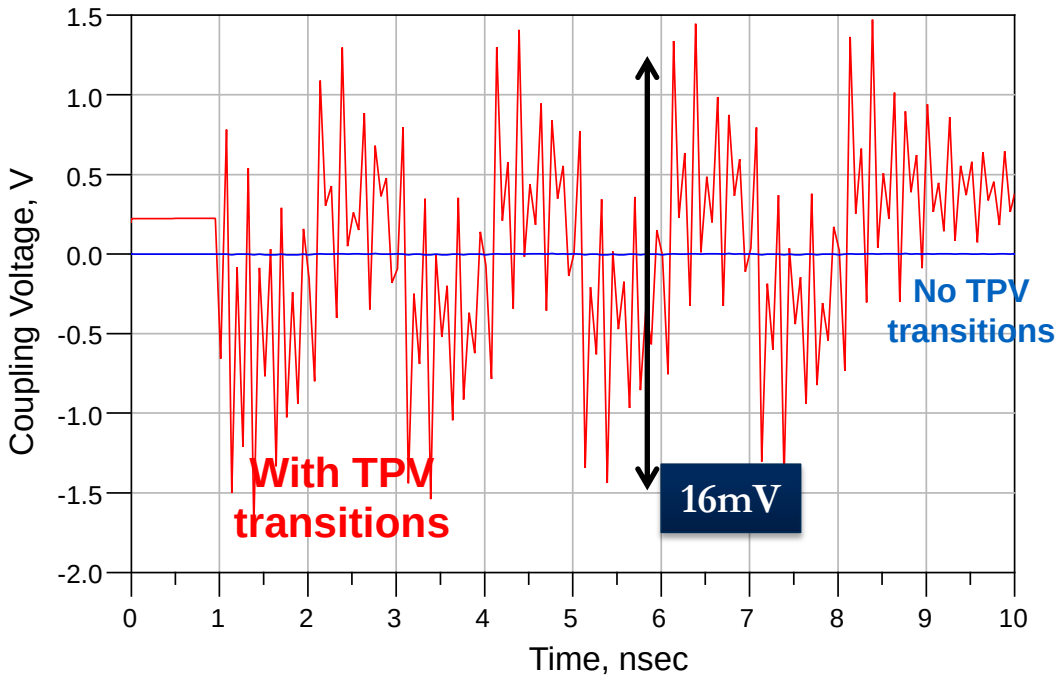


Figure 46: Time domain signal to power noise coupling

The resonance effects were also observed in time domain, manifested as signal-to-power coupling voltage. The coupling noise waveform between signal lines and PDN at the center of the planes is shown in Figure 46. For the 8 GHz input, the coupling noise between the microstrip signal channel and the P/G plane was negligible in the absence of TPVs. However, the glass interposer with via transitions showed about 16 mV noise due to the coupling with through via discontinuities. Therefore, when signals were transferred

through the through- package- vias away from the reference ground plane, the quality was greatly degraded at the power and ground resonance frequencies. Hence, investigation of resonance suppression schemes is a critical need and is described in detail in the next chapter to enable good signal and power integrity in 3-D glass interposers.

3.3 Summary of power delivery investigation in double-sided 3-D glass interposers

a. Power Delivery Resonances in 3-D glass interposers

- A simplified multi-port method was established to simulate the fundamental resonance mechanisms in 30μm ultra-thin, 3-D glass interposers. The self-impedance PDN profile was obtained by connecting S-parameter blocks with lumped parasitic values. The results were compared to conventional 2-D glass packages having fully-populated solder ball grid array (BGA) connections.

- At the mode resonance frequencies, additional resonances in the self-impedance 3-D PDN profile were observed near 7.3 GHz for the 3-D glass interposer package, due to the interaction of the increased lateral inductance with the package cavity.

- The additional increased inductance due to 3-D glass interposer packages (0.44nH) was 110 pH, when compared to 2-D glass packages (0.34nH) with fully populated BGAs. Hence, the 3-D glass interposer package PDN design should be designed more carefully when compared to 2-D glass and organic packages.

- System PDN studies with on-chip+interposer+PWB elements suggested that these high-impedance peaks in the PDN profile of 3-D interposer systems were mitigated due to the domination of the on-chip capacitance at GHz frequencies.

- Based on these investigations, impedance suppression methods for all resonances in glass interposers were identified as a critical need, and are thoroughly examined in the next chapter, resulting in a set of design guidelines.

b. Signal Integrity impact due to PDN resonances

- The simulation of wide-I/O channel in 3-D glass interposers was verified to obtain high BW with very low loss (<0.16dB) and parasitic delay (160ps), compared to 3D-ICs. However, the effect of power delivery resonances becomes predominant in external I/O channels due to the return path discontinuity that increased SDN-PDN coupling.

- Full-wave EM solvers were used to simulate the effects of power delivery resonances on signal interconnections in 3-D interposers. The modeling results of the signal insertion loss variations correlated well with the changes from power-ground plane impedance in frequency domain.

- The signal integrity of 3-D interposers can be improved using P/G resonance suppression methods to mitigate the effects of discontinuities, which will be discussed in the next chapter.

CHAPTER 4

DESIGN AND ANALYSIS OF 3-D GLASS INTERPOSER PDN RESONANCE SUPPRESSION SOLUTIONS

The P/G resonance mechanisms and their interactions in 3D double-sided glass substrates were modelled from first principles in Chapter 3, arriving at a set of quantified challenges in power delivery network design. This chapter describes the modeling and design of effective resonance suppression methods to eliminate these challenges, arising from both the glass as a highly insulating substrate material and the added lateral PDN path.

4.1 Overview of PDN resonance suppression solutions with 3-D glass interposer packages

The biggest fundamental challenge in achieving effective power delivery in 3-D glass interposer packages without resonances is the presence of inductive elements in the high-impedance glass substrate. The primary method to mitigate these impedance peaks consists of strategically placing decoupling elements in the PDN. Several suppression techniques have been demonstrated for lowering the PDN inductance to meet target impedance, based on the supply- ripple voltage requirements [65, 83, 85, 86]. However, the added lateral trace inductance in 3-D interposers leads to frequency-dependent Equivalent-Series-Inductance (ESL) over and above the ESL of the decoupling capacitors. Therefore, using such decoupling capacitors in 3-D interposer packages may actually exacerbate the PDN problems at higher frequencies by adding additional P/G

inductance. This chapter describes the research conducted to arrive at a set of design guidelines for decoupling and resonance suppression solutions specific to 3-D glass interposer packages, while minimizing the overall PDN loop-inductance towards effective power delivery.

The 3-D glass interposer package structure provides several benefits in power delivery network design and decoupling methods over organic and silicon interposers: (a) integrated interposer and package PDN simplifying PDN design compared to silicon interposers, (b) increased density of package P/G TPVs and chip-level C4 interconnections compared to organic packages, (c) the ability to integrate on-package decoupling capacitors that require higher temperature processing than possible with organic interposers, and (d) thick power and ground (P/G) planes (5-8 µm) on an ultra-thin package core (30 µm) to minimize impedance compared to single-side silicon interposers.

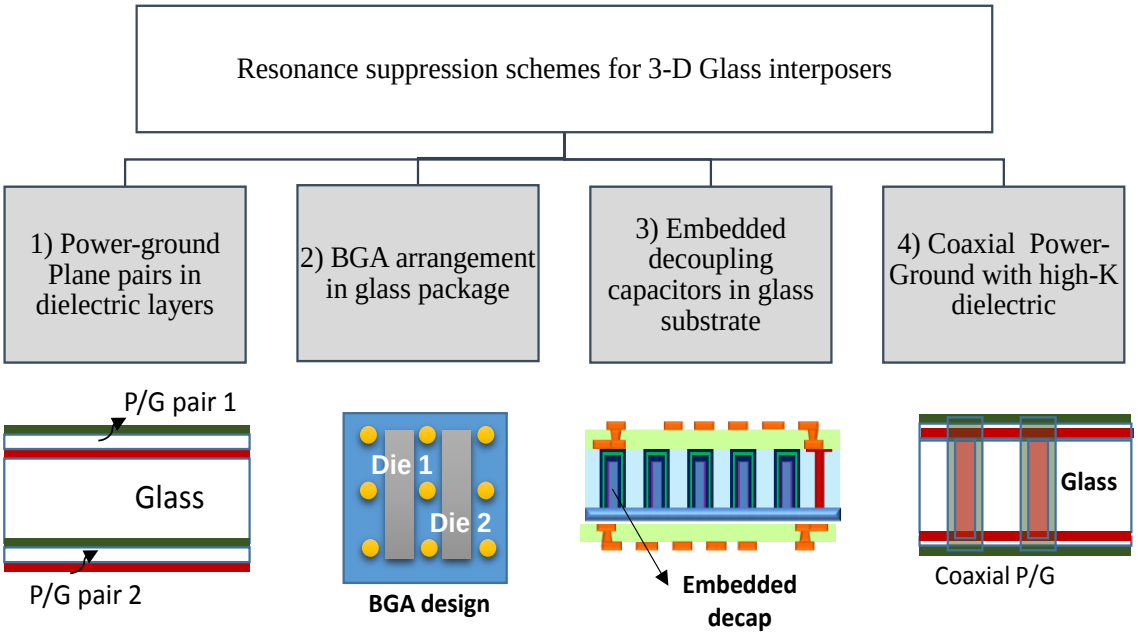


Figure 47: Resonance suppression schemes studied in this dissertation

An overview of suppression methods examined in this chapter is presented in Figure 47. This dissertation studies important design solutions, particularly suited for ultra-thin, 3-D glass interposers, using (1) power-ground plane pairs in dielectric layers, (2) BGA arrangement in the double-sided package. In addition, two fundamentally- new resonance dampening solutions are introduced to provide capacitance within the 3-D glass substrate using: (3) Embedded decoupling capacitors and (4) Coaxial power-ground with high-K dielectric. The final section of this chapter compares these methods in terms of their target resonance frequencies, and formulates design guidelines to achieve the target impedance till 10 GHz, applicable to both mobile and high-performance applications.

4.2 Resonance Suppression using plane pairs in dielectric layers

This section studies the PDN design of 3-D glass interposers having power-ground layers across the build-up layers fabricated on the top and bottom surfaces of the glass core substrate, for improved power integrity. This approach provides distributed capacitance very close to the die, with low-ESL and without additional space requirements. The power-ground pairs were interconnected between one-side of the glass core to the other side using parallel through-vias at fine pitch (30μm) with negligible total (~2 pH) parasitic inductances. A schematic view of the glass substrate cross-section and port locations used in this study is shown in Figure 48. The P/G plane stack-up was chosen to be symmetrical to minimize warpage during fabrication and chip assembly.

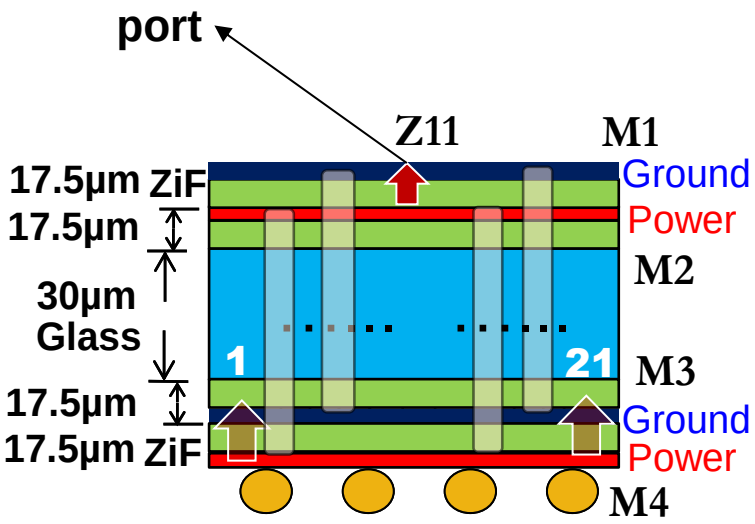


Figure 48: Cross-section of P/G plane pairs on glass interposers across build-up layers

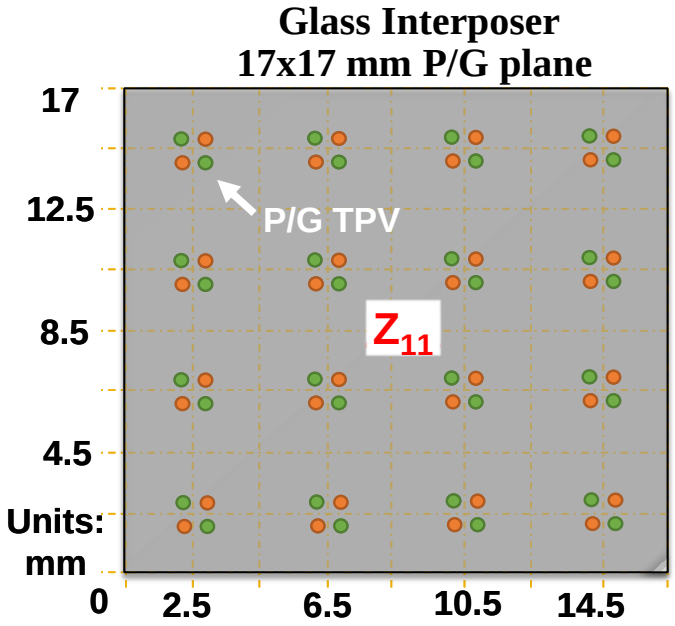


Figure 49: Top view of Via Location for P/G planes on Build-up Layers

The loop inductance of the PDN was reduced by connecting uniform TPV hole locations in-plane as shown in Figure 49. A simplified P/G plane stack-up on ultra-thin 30µm glass cores was previously analyzed in chapter 3 to mitigate the PDN loop inductance. The stack-up was developed with Zeon-ZIF polymer that was introduced in Chapter 3. The PDN structure design was extended to explore two types of build-up polymer thicknesses with: (a) 17.5µm ZIF and (b) 5 µm ZIF. In addition, glass substrates having a thickness of 100 microns, laminated with polymer of thickness 17.5µm were analyzed to determine the impact of the glass core thickness on the PDN impedance profile. Full-wave simulations were performed to compare the PDN impedances and resonances of the individual configurations.

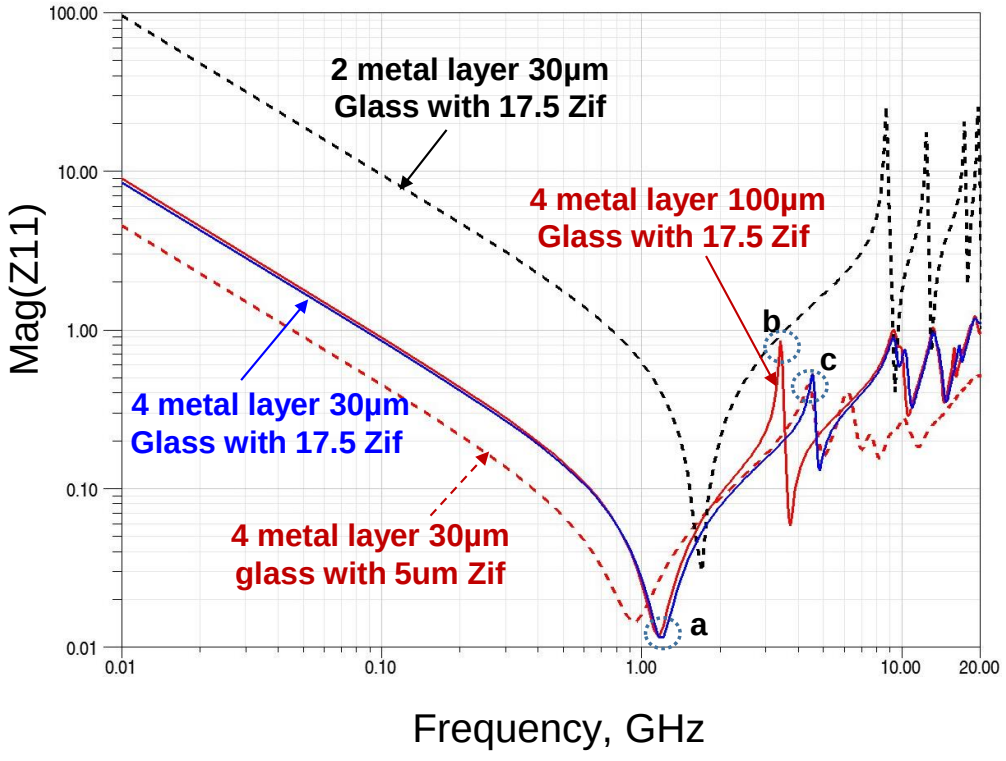


Figure 50: Self-impedance comparison of PDN with four metal layers

The self-impedance profiles were simulated at the center of the top metal layer for different P/G configurations, and are plotted upto 20 GHz in Figure 50. The four-metal-layer P/G plane structure had 10X lower impedance than the two-metal-layer stack-up, across all frequencies that were considered. Among the different four-metal layer stack-up variations, the magnitude of anti-resonant peaks were suppressed more for the glass core with a thickness of 30 µm ('c' in Figure 50), compared to the glass with a thickness of 100 µm core ('b' in Figure 50) due to the additional capacitance between M2 and M3 metal layers. However, similar series resonance frequencies ('a' in Figure 50) were observed in both glass thicknesses with a fixed build-up dielectric layer thickness of 17.5µm, which is attributed to the identical planar capacitance between M1-M2 and M3-M4 in both cases.

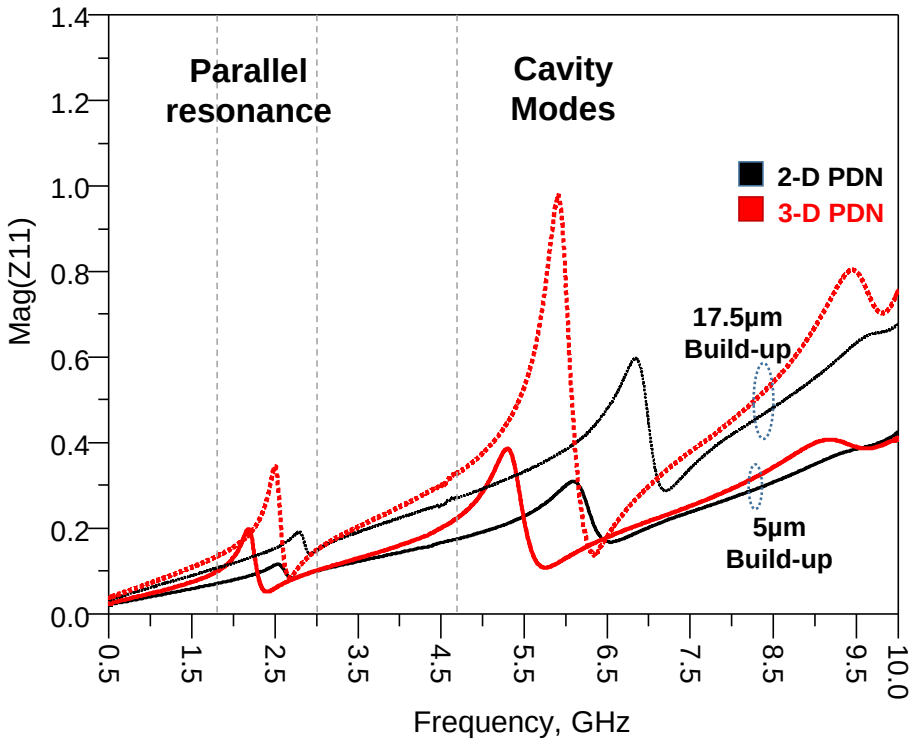


Figure 51: Self-impedance comparison of 3-D PDN build-up thickness variation

While the overall impedance magnitudes of the four-metal P/G plane structures were 10X lower than the two-metal structures at all frequencies under consideration, an additional parallel resonance was observed at lower frequencies near 2.5 GHz, due to the interaction of the lateral inductance of the planes with the capacitance between the build-up metal layers (M1-M2). This effect was further examined in Figure 51, labeled as parallel resonance, which compares the impedance profiles of four-metal layer 2-D and 3-D PDN. These resonances can be minimized by optimizing the placement of the P/G TPVs used to interconnect the planes. The use of thinner build-up layers (1-5 μm) was also shown to provide complete suppression of P/G resonances across a wide-frequency range.

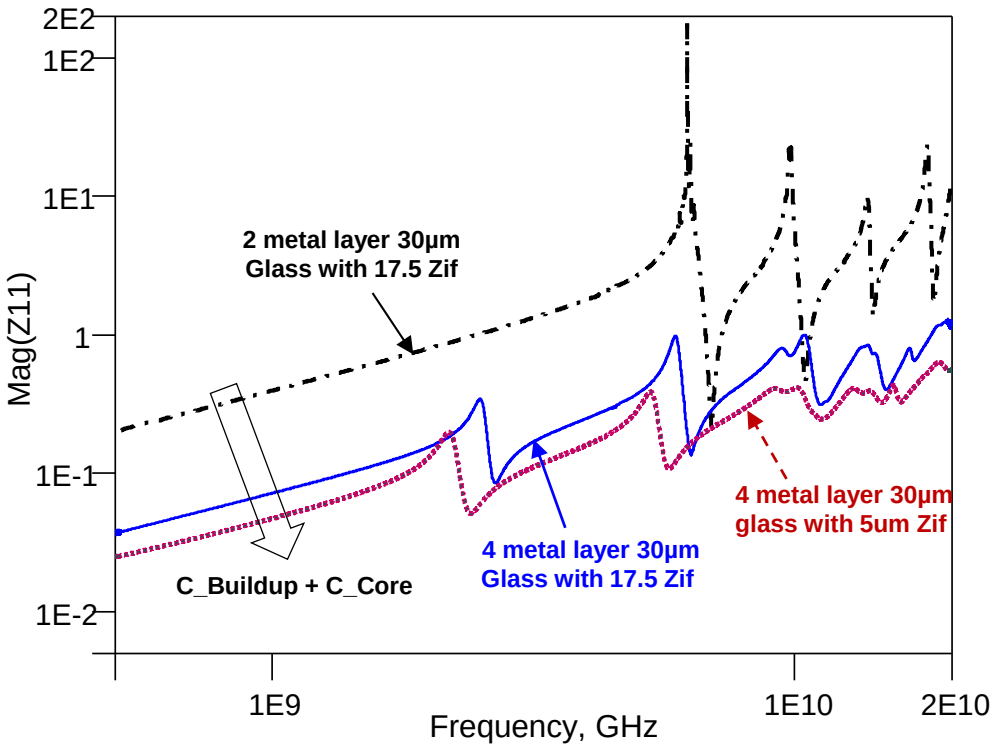


Figure 52: Self-impedance comparison of 3-D PDN of package stack-up with ideal PWB

This study was extended to compare the self-impedance profile of the complete system PDN for two-metal and four-metal P/G stack-up of 3-D PDN, as depicted in Figure 52. The parallel modes were studied by grounding the PWB and VRM locations. The proposed four-metal P/G planes were found to reduce the magnitude of the high-impedance peak in 3-D interposers from 180Ω to 0.9Ω, providing effective mitigation of P/G resonances in 3-D interposers. The overall magnitude to the Z11 impedance profile was also reduced by 10-50X down to hundreds of mΩ, which can meet the target impedance requirements of mobile applications. This method should be combined with discrete decoupling capacitors to further reduce the impedance magnitude at lower frequencies below few MHz.

4.3 Resonance Suppression Design using BGA arrangement

This section analyzes the impact of design variations from solder BGA placement on the PDN self-impedance profile of 3-D glass interposer packages. Different types of BGA arrangements that were studied to evaluate their corresponding resonance frequencies are illustrated in Figure 53, based on the number and location of BGA pins connecting to the printed wiring board (PWB). The first variation, with finer BGA pitch (‘type c’ from Figure 54) was designed to have the same number of P/G BGAs as a 2-D interposer with full BGA array (‘type a’ from Figure 54). Such a configuration, termed as “increased pitch 3-D PND” can be achieved by employing finer-pitch BGAs. The second variation (‘type d’ from Figure 54) was designed to allow access to center of the interposer by splitting the bottom die into two smaller dies while having a reduced number of BGAs compared to the 2-D interposer. This split die approach to 3-D (termed

"Split die 3-D PDN) enables the study of the impact of changing the number of P/G BGAs.

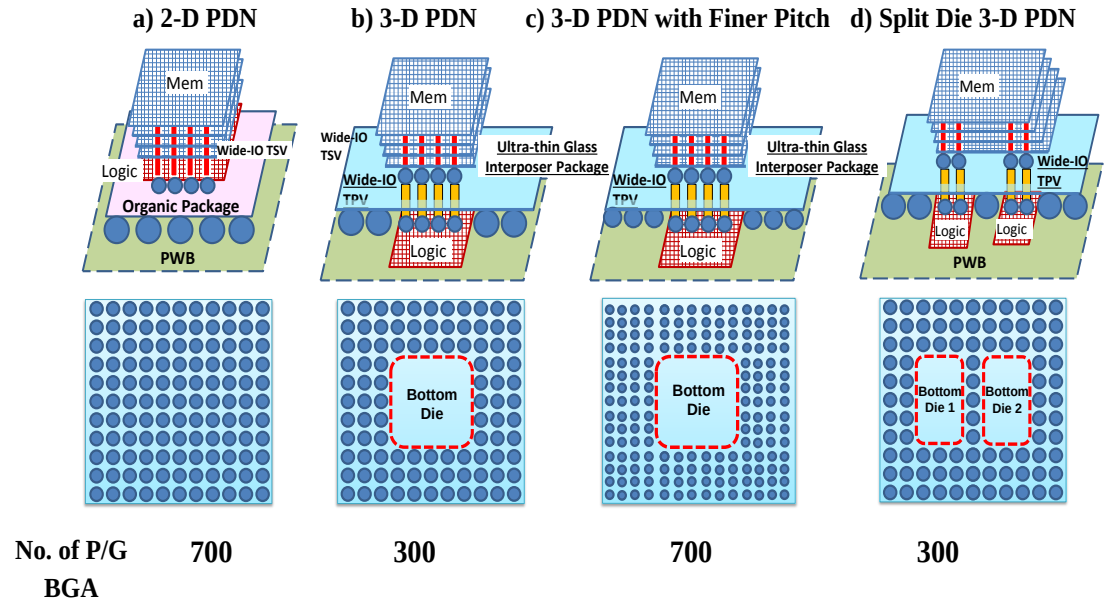


Figure 53: Various BGA arrangements studied in 3-D glass interposers

The port assignment locations and number of P/G BGA pairs for each configuration are shown in Figure 54. The impact of self-impedance from two alternate BGA arrangements based on die-placement was compared with 3-D PDN, without the on-chip P/G grid and the PWB. The high-impedance anti-resonant peak observed in 3-D PDN was suppressed effectively using the two approaches described in Figure 7c and 7d. The magnitude of resonance suppression using the split die configuration ('type d') was much larger than using the finer-pitch 3-D PDN ('type c') approach. Thus, the lateral trace inductance had a much larger impact on the self-impedance profile compared to the inductance of parallel BGA's. Hence, the use of multiple smaller dies to facilitate placement of P/G BGAs at the center of the interposer, minimizes IO-PDN resonances at

the package level much more than using a single large die. This technique was effective in reducing the anti-resonant peaks above 5 GHz. However, inductive impedance below 5GHz could not be suppressed by this method due to the inherent package parasitics.

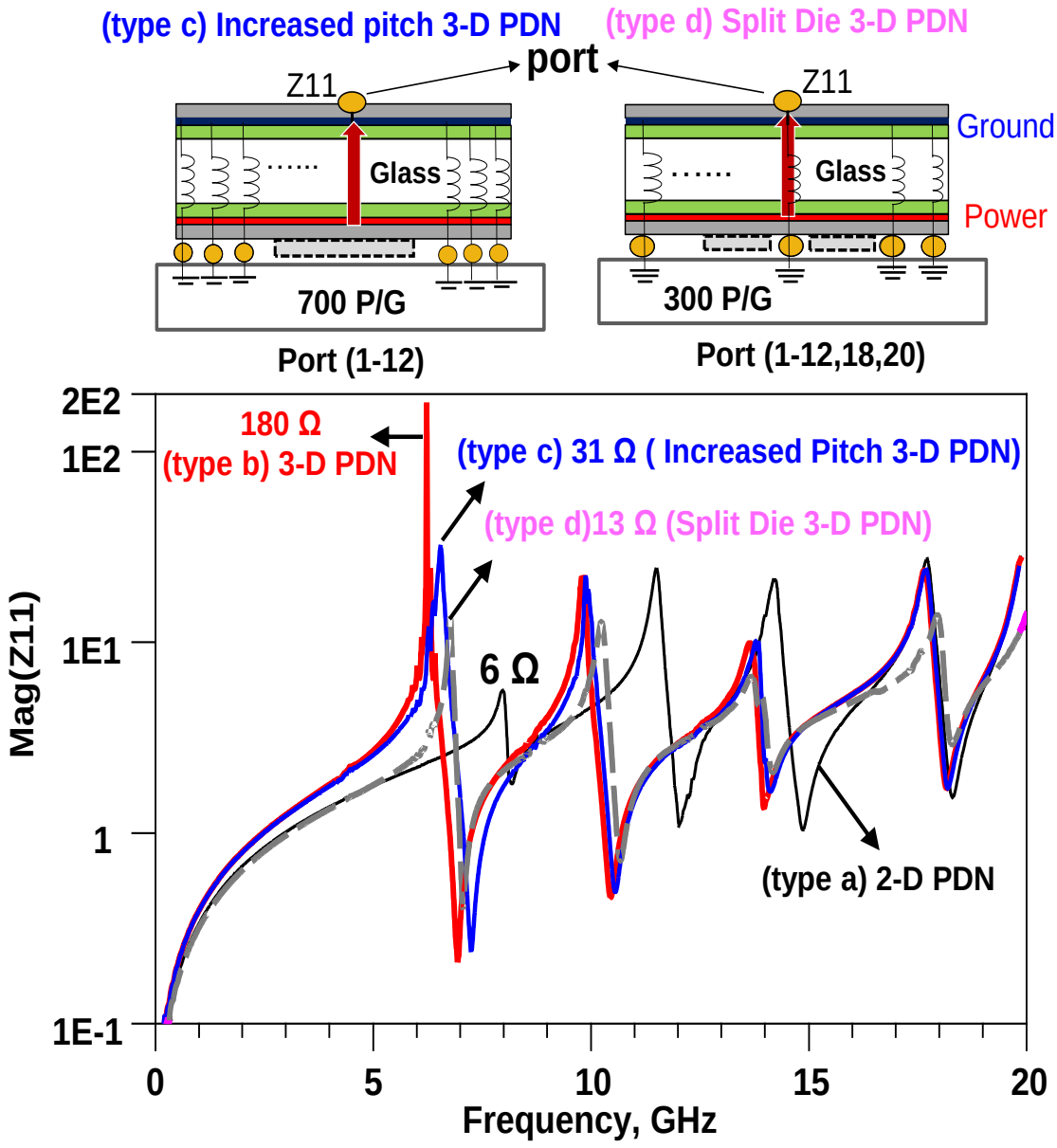


Figure 54: Comparison of BGA placement schemes

4.4 Resonance Suppression Design using Decoupling Capacitors in 3-D glass interposers

The selection and placement of decoupling capacitors to reduce PDN inductive impedance is a critical element in PDN design. This section analyzes the effect of decoupling capacitors and their placement on the PDN impedance of 3-D glass interposers.

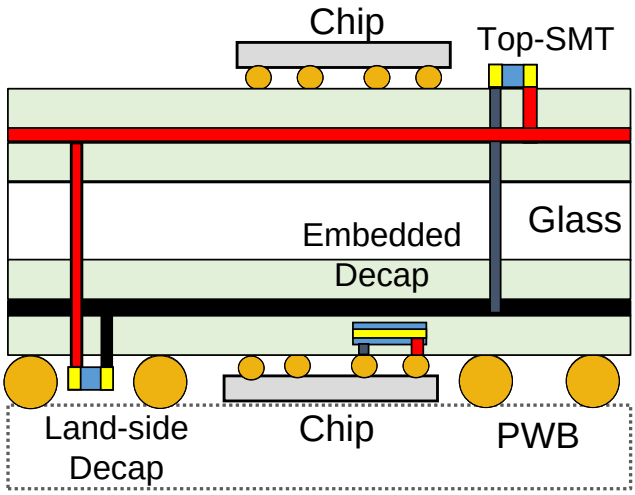


Figure 55: Decap placement in 3-D interposers

Three different locations for integrating decoupling capacitors in the 3-D interposer package are illustrated in Figure **55**. The land-side placement of discrete capacitors at the underside of the package is restricted in double-sided interposers due to the presence of the die and the BGAs. The ESL for different values of surface mount technology (SMT) capacitors is presented in Figure 56. Based on this analysis, the SMT-based discrete capacitors mounted on the top side of 3-D interposers were ineffective at higher frequencies greater than 0.1 GHz due to their longer power delivery path and high

equivalent series inductance (ESL), as shown in Figure 55. Therefore embedded decoupling capacitors using ultra-thin integrated passive devices (IPDs) or thin-film technologies [76, 87] are considered the best choices to provide effective high-frequency decoupling.

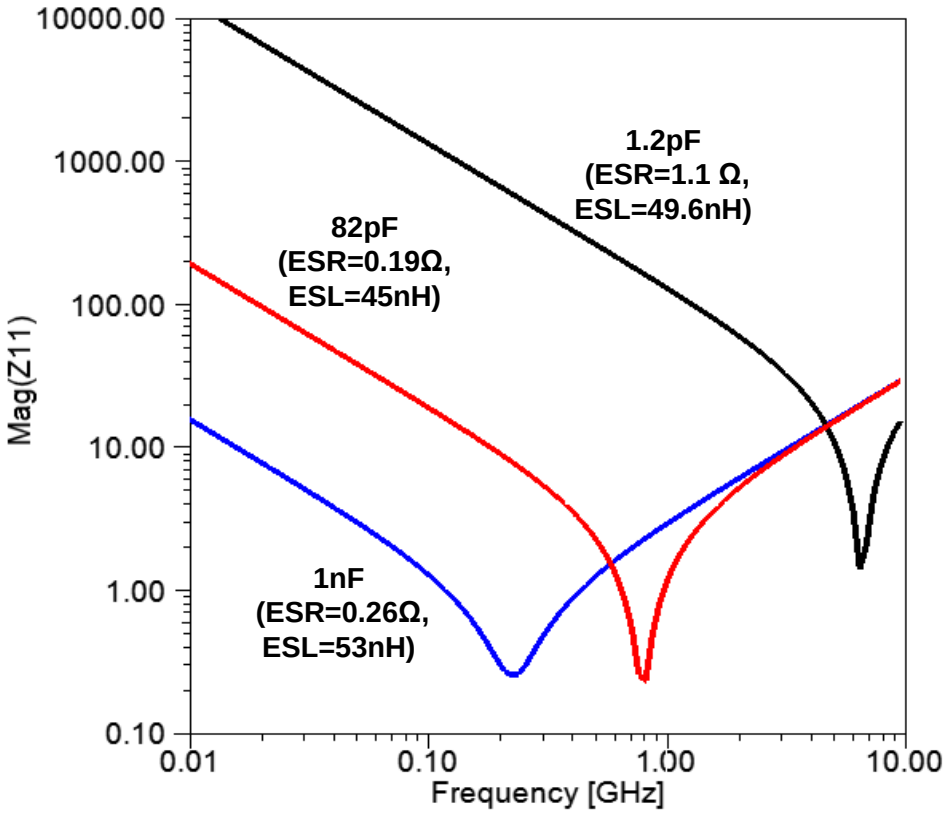
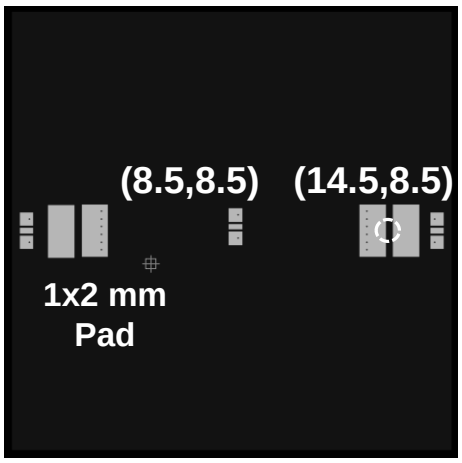


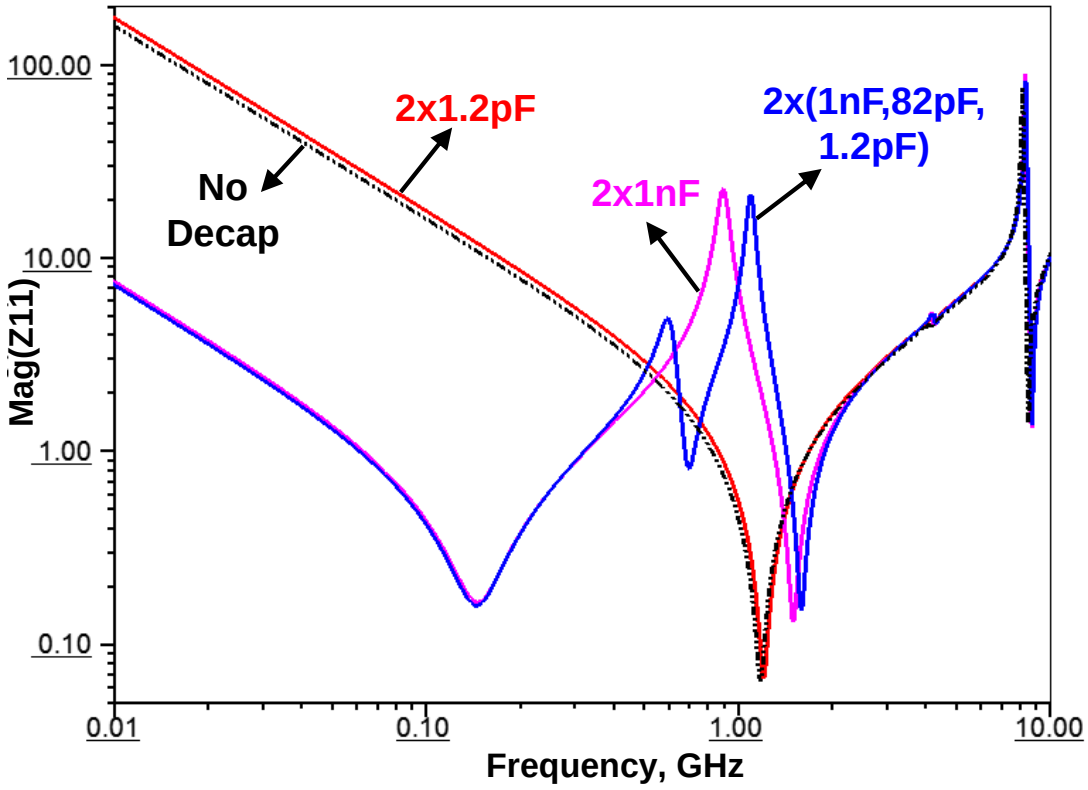
Figure 56: ESL comparison of SMT-type Decoupling Capacitors

The ESL-limitations of discrete decoupling capacitors at higher frequencies in glass interposers are illustrated in Figure 57. The simulations were performed using a signal and power integrity tool – SI-wave. As an example, the self-impedance profile of the 3-D interposer PDN was simulated for the placement of 0603 EIA size decoupling capacitors. Smaller size discrete capacitors with lower-ESL (example: 0402 and 0201 size) could be used to suppress higher frequency resonances. However, the loop-inductance due to the

placement restrictions from double-sided die attachment limits the effectiveness of low-ESL discrete decoupling capacitors at higher frequencies beyond 1 GHz.



(a)



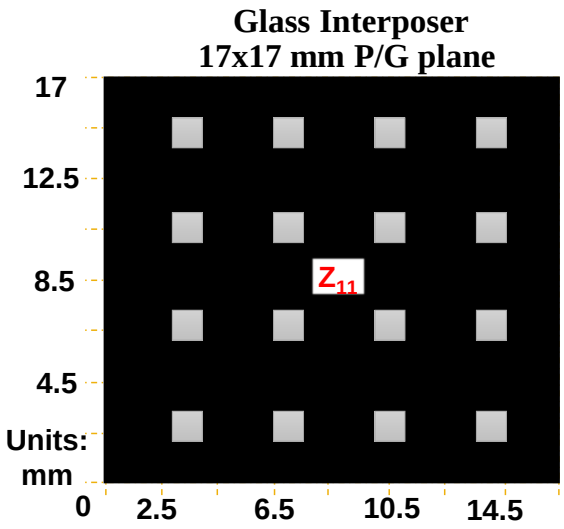
(b)

Figure 57: (a) Placement and (b) Comparison of SMT-type Decoupling Capacitors

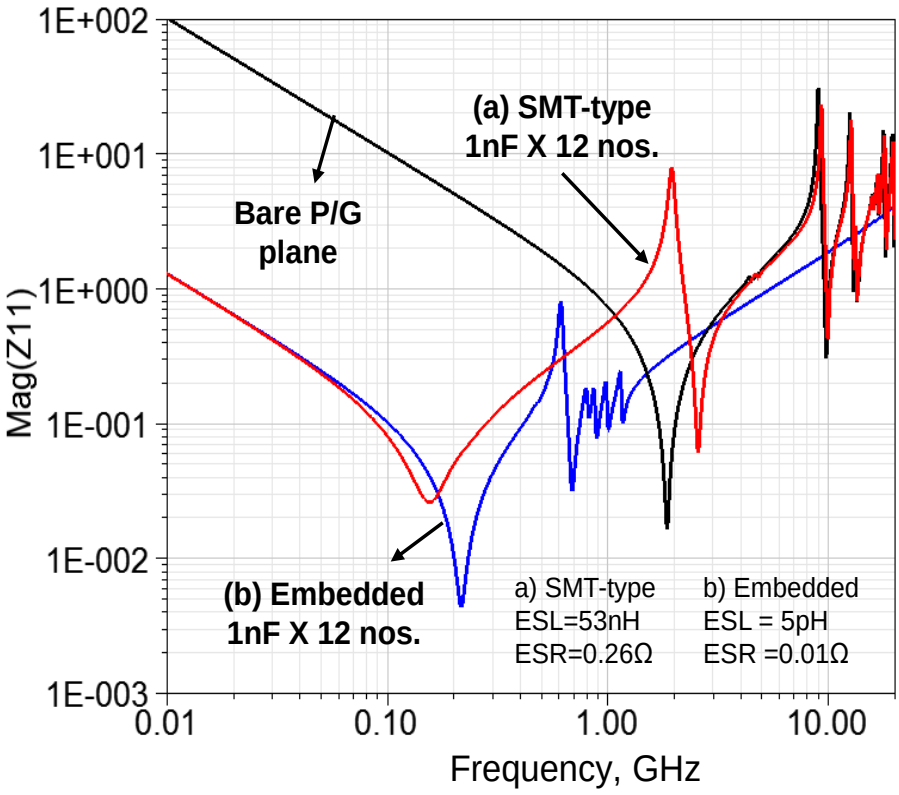
Different capacitor values of 1nF, 82pF and 1.2pF were chosen to study the decoupling impact at multiple frequencies. The capacitors were mounted on SMT-compatible copper pads located at two locations – at a distance of 2.5mm from two non-adjacent edges of the interposer. Capacitors having a value of 1nF were found to be effective in reducing PDN impedance up to 0.1 GHz. There was no improvement in the PDN profile beyond 1 GHz using the 1.2 pF capacitors due to high ESL and loop inductance.

4.4.1 Embedded Decoupling Capacitors in 3-D glass interposers

To address these placement challenges of discrete SMT-based decoupling capacitors, the integration of embedded capacitors in glass substrates was explored. The inorganic nature of glass enables the processing of high dielectric constant materials at high temperatures, similar to silicon interposers. The uniform placement of 1nF embedded and SMT-type decoupling capacitors on a glass package was examined, as seen in Figure 58. While both embedded and SMT-type capacitors provided resonance suppression at frequencies below 0.1 GHz, embedded capacitors were observed to provide lower inductive impedance till 1 GHz. Hence, embedded capacitors can be employed as a miniaturized and more-effective alternative to discrete SMT-type capacitors for 3-D interposer decoupling applications [76].



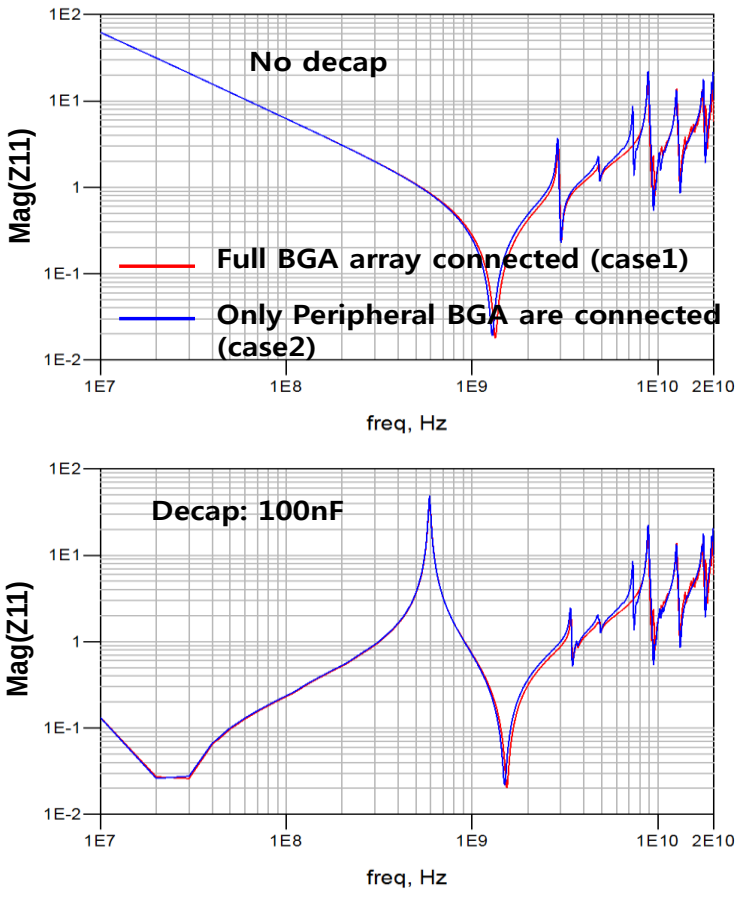
(a)



(b)

Figure 58: (a) Placement and (b) Comparison between Embedded and SMT-type uniform location of 1 nF decoupling capacitors

These studies were extended to compare the effect of embedded capacitors on the self-impedances of 2-D and 3-D glass interposer PDN. The ESL and ESR of decoupling capacitors were neglected to simply the analysis. The Z11 parameter for varying values of decoupling capacitors placed on the PWB are illustrated in Figure 59. The placement of decoupling capacitors on the PWB resulted in a high resonance peak around 600MHz due to interaction between the interposer plane capacitance and the parasitic inductance in both 2-D and 3-D PDN. Similar to the results observed previously in chapter 3, the BGA variations did not have a significant impact on the placement of decoupling capacitors. This illustrates that the PDN system optimization can be performed in 3-D glass interposers in a manner similar to full-array BGA interposers.



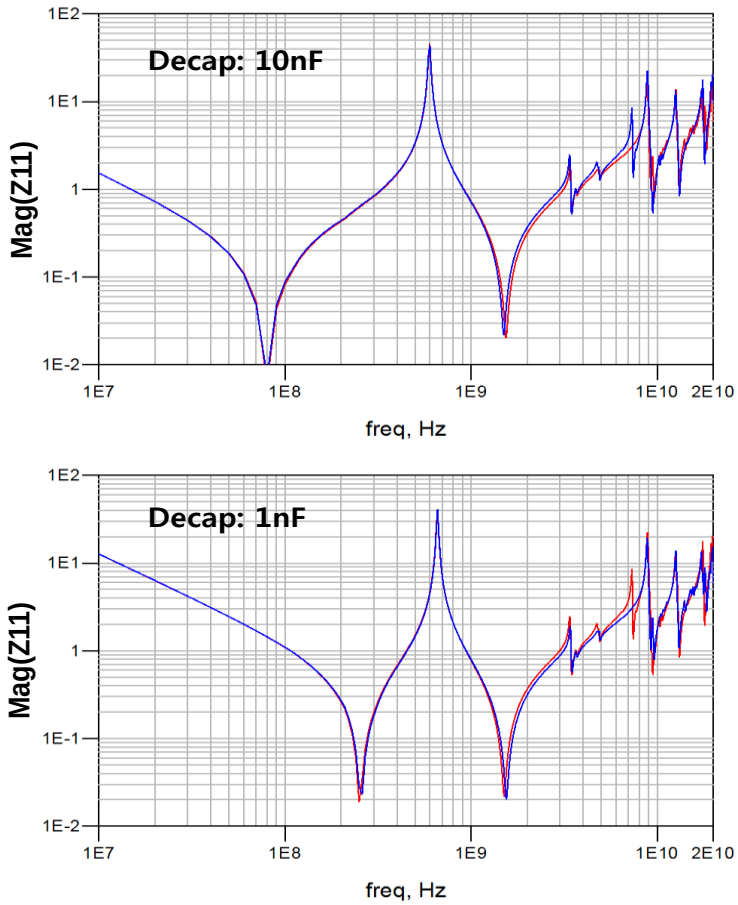


Figure 59: Comparison of Z11 with parametric variation in embedded decoupling

The study was further extended to include the impact of high density thin-film embedded decoupling capacitor (150nF x 4nos.; ESR=10 mohm; ESL=0.15nH) integration into 3D glass interposers at different port locations. Table 6 presents the Z11 magnitude at anti-resonance points and the first resonant frequency of each interposer-package configuration, before and after the placement of embedded decoupling capacitors. The decoupling capacitors effectively reduced the magnitude of impedance and increased the resonance frequency of the 3-D glass interposer PDN. However, additional decoupling locations were needed to achieve the same order of impedance

when compared to corresponding full BGA array packages (2-D PDN) due to added lateral inductance.

Table 6: Magnitude of Self-impedance of 2-D and 3-D PDN due to embedded decoupling capacitors in glass substrates

	No. of P/G BGA	Embedded Decap 150nF X 4nos. (ESR = 10mΩ, ESL=0.15nH)				No. of Decoupling Locations
		Before Decoupling		After Decoupling		
		Mag (Ω)	Freq (GHz)	Mag (Ω)	Freq (GHz)	
2-D PDN	700	5.6	7.8	3.4	8.41	5
3-D PDN	300	70.5	6.2	4.5	8.1	9

4.4.2 Target Impedance Design with hierarchical decoupling elements

The results of decoupling capacitor placement from the previous sub-sections were used to design the PDN package for a typical mobile application [88]. A target impedance of 350 mΩ was used in this study to design the decoupling capacitor network. The different values of decoupling capacitors placed hierarchically on-chip, on the 3D interposer and at the PWB locations are shown in Table 7. The targeted frequency range was from DC to beyond 2 GHz, based on the voltage ripple requirements. The self-impedance of the 3-D PDN system after the placement of decoupling capacitors is presented in Figure 60. The results of this investigation demonstrate that PDN system optimization in 3D interposers can be performed in a manner similar to full-array BGA interposers.

Table 7: Hierarchical Decoupling Capacitor Values

Decap Location	ESL	Capacitance	Port
On-chip	50 pH	5 nF	19
3D interposer package	150 pH	100pF,50nF	21,22
PWB	5 nH	100µF x 4	19-22

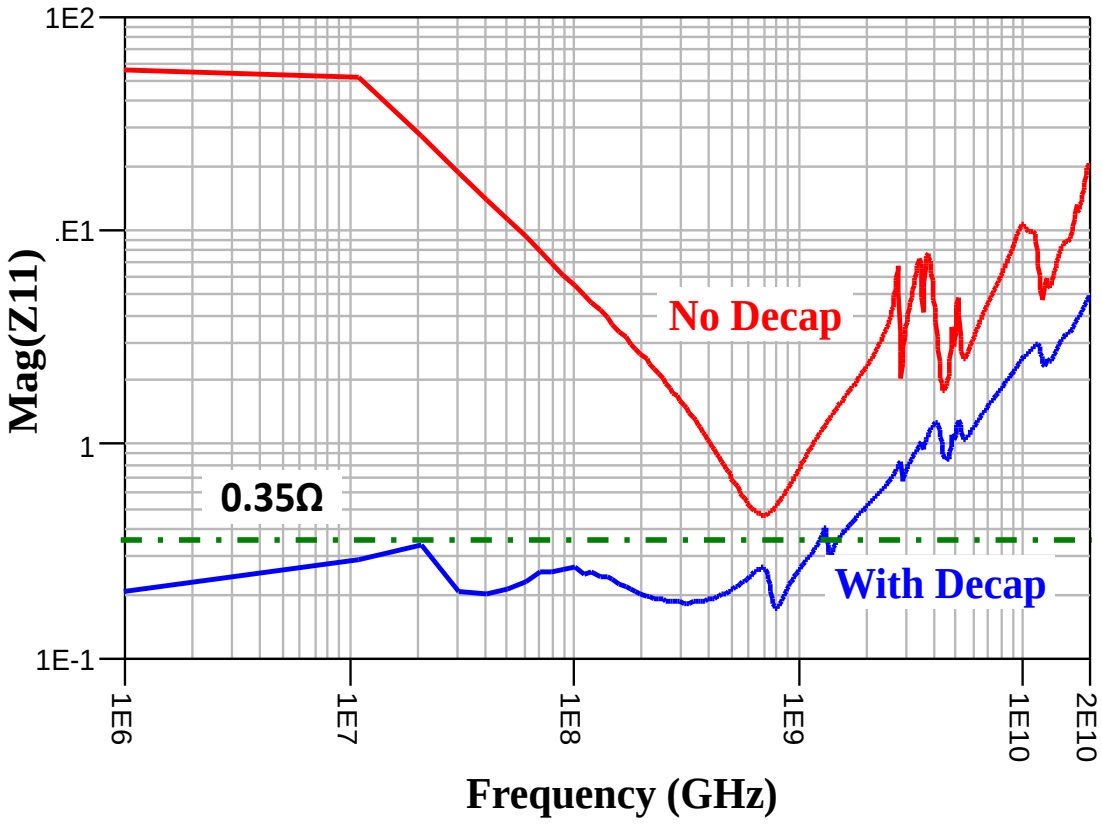


Figure 60: 3D system impedance after decap optimization

4.5 Resonance Suppression Design using coaxial power-ground with Through-package-Vias

This section discusses the investigation of coaxial power-ground with through-package-vias (TPVs) having high dielectric constant liners as an effective method to deliver clean power in a 3D glass interposer package, and provides design and fabrication guidelines to achieve the PDN target impedance. The coaxial TPV structure shown in Figure 15 was simulated using electromagnetic (EM) solvers and a simplified equivalent circuit model, to study via impedance and parasitics. The self-impedance (Z11) of a 3D glass interposer containing the coaxial TPVs was analyzed with variations in (a) via locations, (b) number of coaxial vias, and (c) via capacitance and stack-up, to arrive at optimal PDN design guidelines.

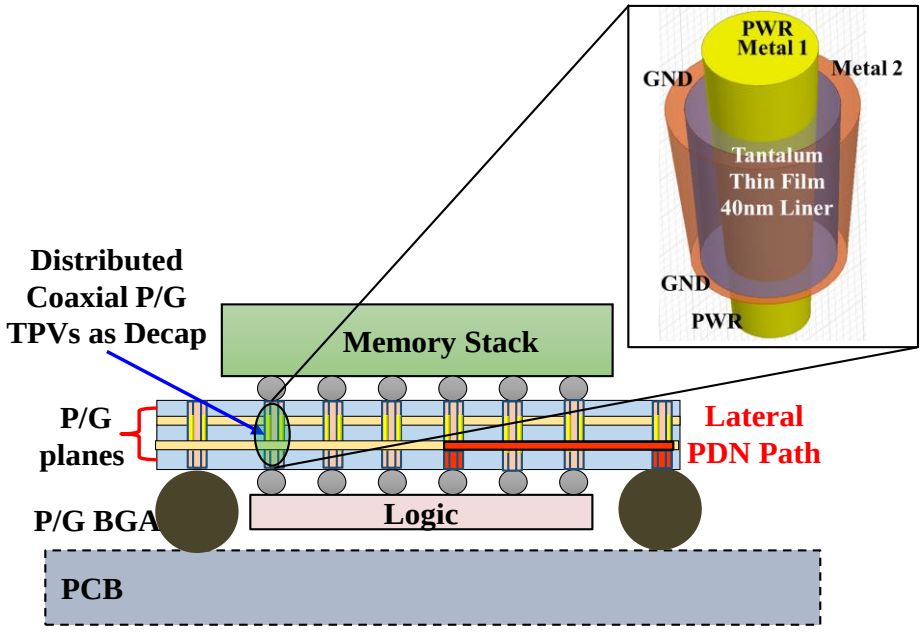


Figure 61: Coaxial Power-Ground Design - System Overview

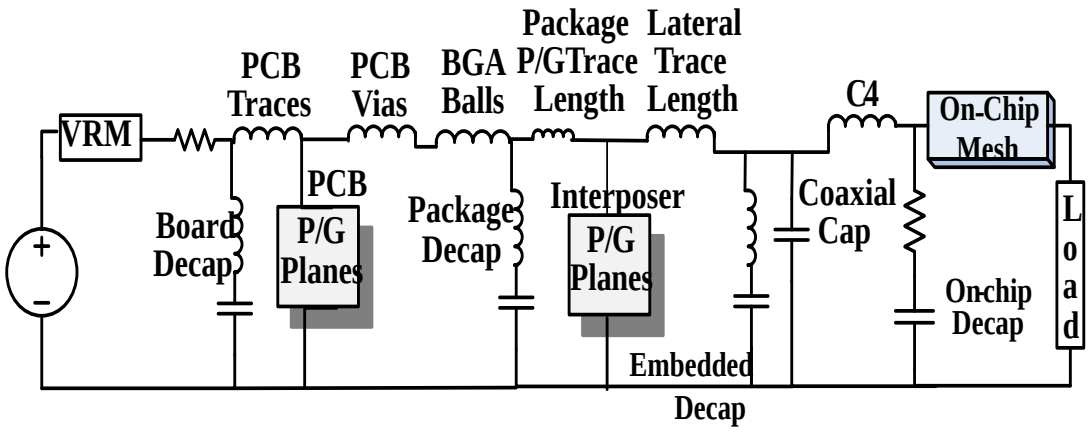


Figure 62: Schematic Diagram of 3D interposer PDN with coaxial P/G TPVs

4.5.1 Electrical Modeling of Coaxial P/G TPVs

This sub-section examines via parasitics for different coaxial TPV process methods and stack-ups, and presents a simplified circuit model to analyze coaxial via interconnects. The parasitic properties of the coaxial vias most critical to PDN design, including the inductance, capacitance and total via impedance were analyzed. Both analytical equations and an electromagnetic solver (Q-3D) were used for this parametric analysis. The negligibly small resistances of thick coaxial vias were not considered in this analysis. Integration of high-k thin film materials such as tantalum oxide and barium titanate between the inner conductor and outer shell of coaxial TPVs in an ultra-thin glass substrate was studied to provide up to 50x higher via decoupling capacitance. Figure 62 shows the electrical block diagram of the 3D interposer PDN including coaxial TPVs.

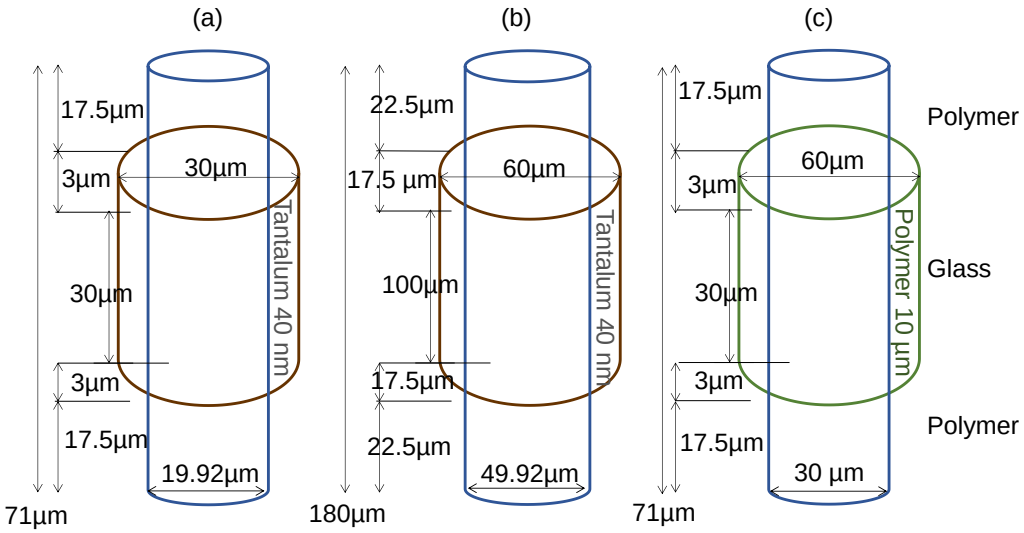


Figure 63: Co-axial Via Dimensions considered in this Study - 40nm tantalum oxide liner with (a) 30µm Glass thickness (b) 100µm thickness, 15µm polymer liner with (c) 30µm glass thickness

Table 8: Summary of coaxial via capacitance

Liner material	ε	Glass Thickness (µm)	Theoretical Value (pF)	Q3D (pF)
Tantalum Oxide	25	30	12.4	12.7
		100	117	120
Polymer	3.01	30	0.0117	0.018

Table 9: Summary of coaxial via loop inductance

Glass Thickness (µm)	Outer Radius (µm)	Inner Radius (µm)	Theoretical Value (pH)	Q3D (pH)
30	10	9.96	0.028	0.022
100	25	24.96	0.042	0.032
30 (polymer)	25	15	3.63	4.7

Three coaxial TPV physical configurations were chosen, based on process feasibility studies, as shown in

Figure 63 Figure 63. Two variations of total TPV height (71 µm and 180 µm) in ultra-thin glass substrates (including dielectric and glass sections) was considered with both moderate-K (Tantalum oxide) and low-K (polymer) dielectric liner configurations. The target metallization thickness was defined to be 5 µm. The simplified analytical expressions for capacitance and loop inductance per unit length of a coaxial via were defined from literature as follows:

$$C_L = \frac{2\pi\varepsilon_0\varepsilon_r}{ln\left(\frac{D}{d}\right)} \qquad F/m$$

$$L_L = \frac{\mu}{2\pi}\ln(D/d) \qquad H/m$$

D is the outer via radius

d is the radius of the inner via

$\varepsilon_0, \varepsilon_r$ is the permittivity of free space and TPV liner

µ is the permeability

A summary of individual capacitance values that were extracted for coaxial vias is shown in Table 8. The maximum capacitance values were achieved with the 100µm glass vias having the tantalum oxide liner, due to the highest capacitance density and surface area. The details of coaxial TPV loop inductances are tabulated in Table 9. The loop inductance of the P/G via with tantalum oxide liner was extremely small due to the thin coaxial liner compared to the loop inductance of a polymer based coaxial TPV. These results indicate the potential for effective PDN design with the proposed P/G TPV configurations.

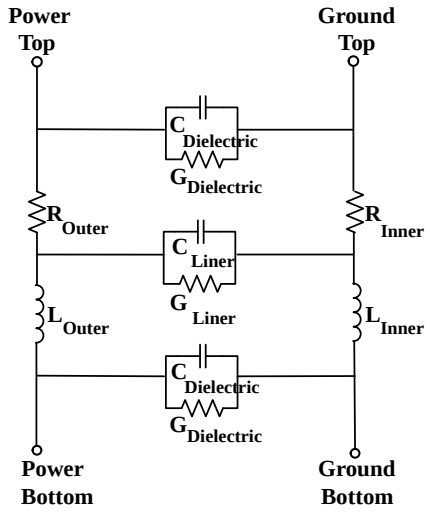


Figure 64: Circuit model for Coaxial P/G Glass TPVs

Based on the extracted values, a simplified equivalent circuit model for glass TPVs was constructed as shown in Figure 64. The dominant capacitance was attributed to the thin high-K liner material sandwiched between the power and ground conductors. The theoretical value of the coaxial P/G vias was computed to be in the several tens of pico farads. The impedance profile of a single P/G coaxial TPV from different configurations was simulated using a full wave EM solver (HFSS) as shown in Figure 65. The self-impedance was measured between via pads of the top two metal layers. It was seen that lowest impedance was observed with 100µm glass thickness coaxial TPV due to its larger surface area and length of the capacitor, followed by the ultra-thin 30 µm TPV. The impedance of polymer- based coaxial vias were several orders of magnitude higher than the other configurations, with smaller capacitive values due to larger separation between the metal plates. The effective capacitance of coaxial vias could be increased by connecting a number of the coaxial P/G vias in parallel, similar to the configuration

adopted in current silicon interposers. The higher capacitance vias exhibited decoupling at lower frequencies, enabling selective tuning to meet the target impedances.

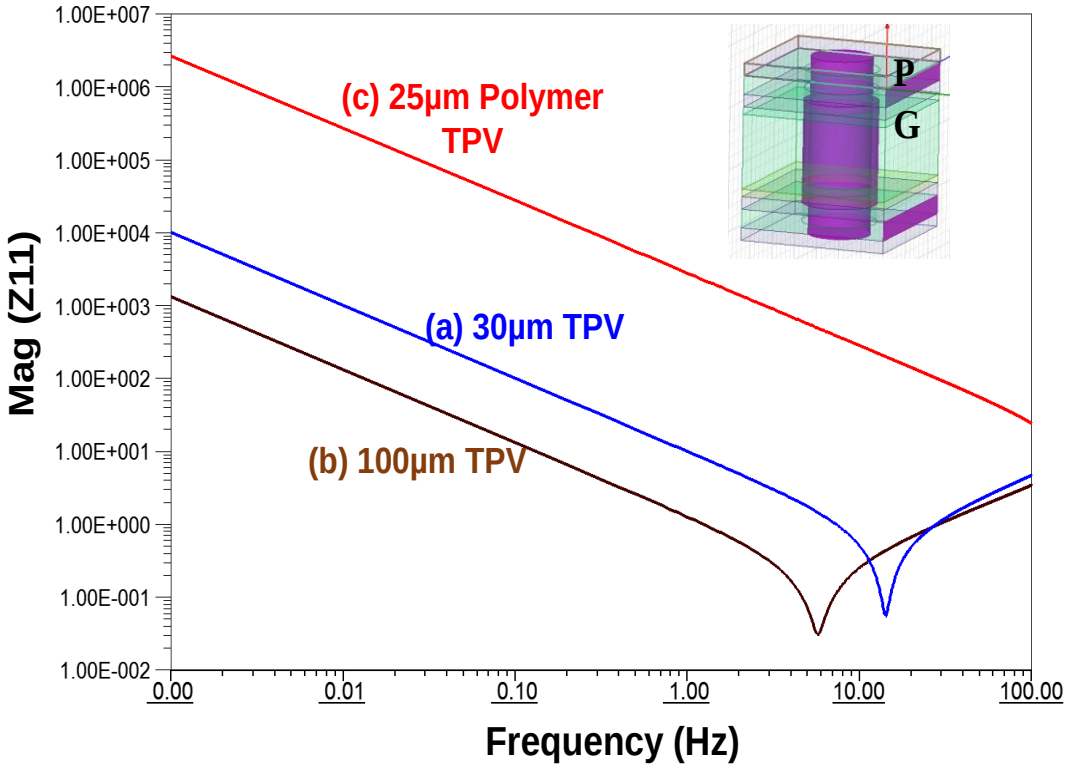


Figure 66: Self-Impedance profile of single P/G coaxial via

4.5.2 Simulation of PDN self-impedance with P/G Coaxial TPVs

This sub-section evaluates the design benefits of the proposed coaxial vias for PDN design through the comparison of PDN self-impedance variations due to the addition of coaxial TPVs.

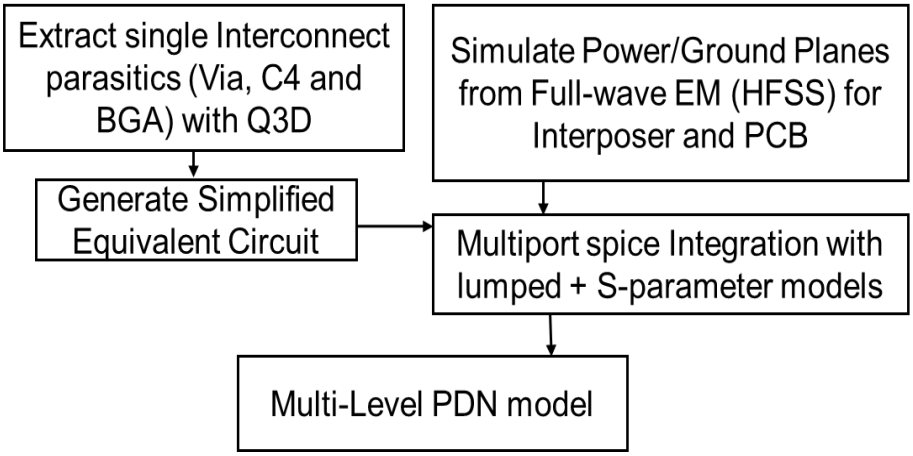


Figure 67: Flow Chart for the segmented PDN approach.

The simulated system configuration consisted of a four-metal layer glass interposer including coaxial P/G TPVs. Since modeling the entire PDN including vias and PWB interconnects is challenging due to long simulation times, a combination of segments from full-wave simulations and spice integration was used to perform PDN system analysis. This method, described in detail in [4] and Figure 67, was used to compute the total PDN impedance profile in frequency domain, through the integration of distributed ports across the package and PWB planes. The PDN impedance of individual package and PWB planes was modeled using a 3D EM solver (Ansys HFSS). The multi-port P/G plane impedance models were then integrated with BGA and via lumped parasitics at appropriate ports depending on the configuration. Figure 12 presents numbered port locations for the BGA and coaxial via group net placements. In this PDN study, the interposer was considered to be always connected to the PWB through BGAs and vias, in order to model the impact of TPVs and BGA variations. The assumptions for BGA placement in this study were the same as [4] and Table 6, and the vias were placed from ports 1-20 on both the interposer and PWB, with the impedance profile studied at port 19 of the interposer.

Table 10: Dielectric properties of substrate materials

Material	Dielectric Constant, ε@ 1MHz	Loss tangent, tan δ
Borosilicate Glass	5.3	0.004
Polymer Laminate	3.01	0.005
Tantalum oxide	25	0.001

Table 11: BGA Port Configuration

Configuration	No. of P/G BGAs	PKG to PWB port connections	L(pH) /port
2-D PDN with Full BGA array	700	1-16	7.69
3-D PDN	300	1-12	4.7

4.5.3 PDN self-impedance variation with P/G Coaxial TPVs

Referring back to the investigations discussed in Chapter 3, the loop inductance of the double-sided 3-D interposer package was found to be trace-dominated and the reduction of interposer P/G BGAs due to the bottom die placement had minimal impact on the system PDN self-impedance at low frequencies.

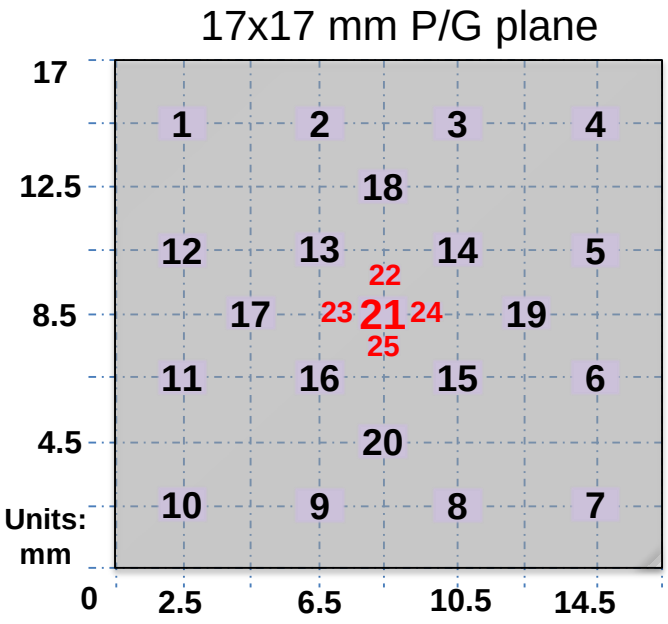


Figure 68: Port assignment for coaxial power-ground study

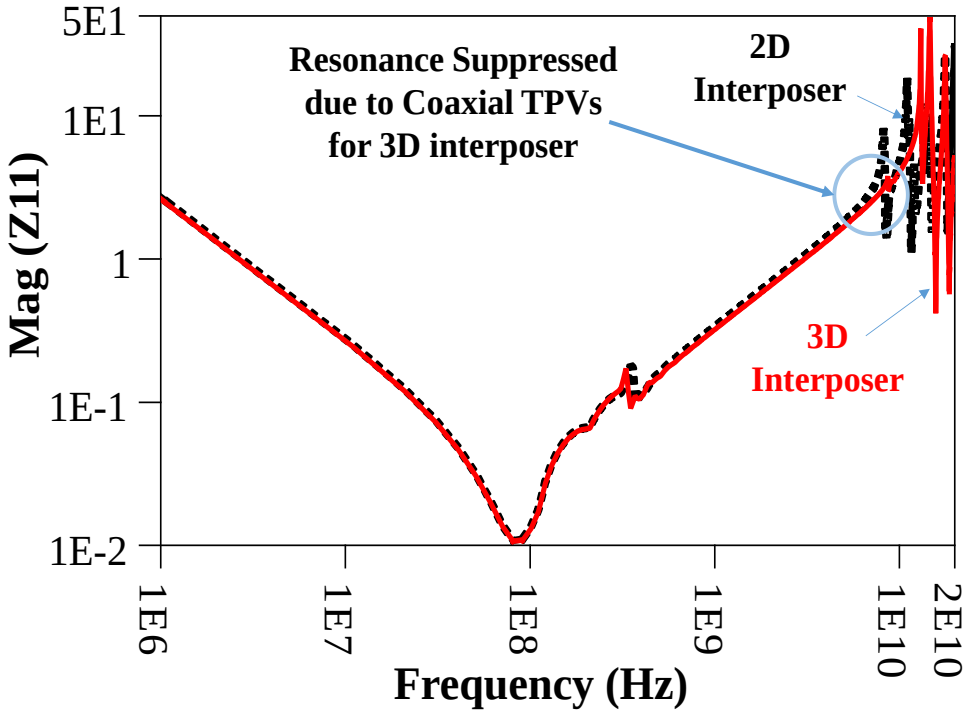


Figure 69: Resonance suppression due to coaxial vias

A comparison of the PDN profile before and after the addition of decoupling vias is presented in Figure 70. Decoupling vias with a capacitance of 30pF per via were considered in this study. Based on the system configuration, 2000 of these coaxial vias were assumed to be present in parallel, as part of the interposer PDN. Both the full-array interposer and 3D interposer PDN had shifted series resonances occurring at 100 MHz due to the series coupling between the decoupling capacitance and the plane capacitance. The addition of decoupling vias completely suppressed the 3D interposer resonances around 10 GHz and shifted the resonance to lower frequencies, demonstrating a clear benefit of using coaxial TPVs in power delivery design.

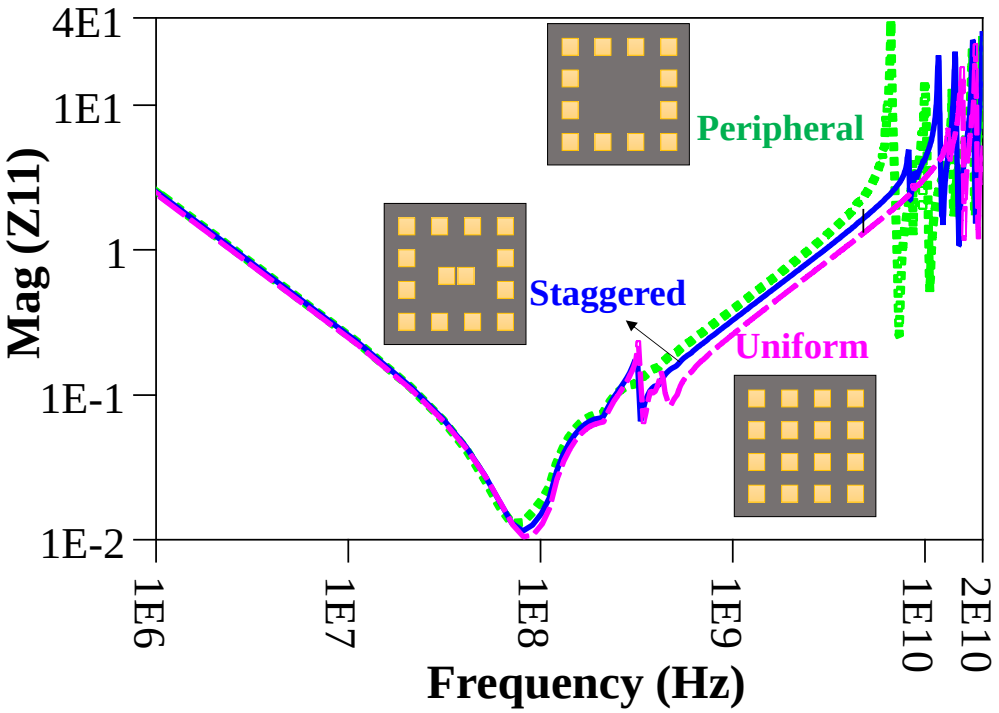


Figure 71: PDN impact due to via placement variations

4.5.4 PDN self-impedance variation with P/G Coaxial TPV Placement

The comparison of the PDN profiles based on the variation of decoupling via distribution in the 3D glass interposer is presented in Figure 71. Three types of via arrangements were considered based on the coaxial via distribution; (a) uniform distribution across the entire P/G plane, (b) Staggered distribution at the center and periphery, and (c) coaxial vias on the periphery only. The same number of decoupling vias (2000) were used in all three arrangements, with variations only in via distribution as shown in Table 12. The uniform distribution of coaxial vias achieved the lowest impedance profile, followed by the staggered and peripheral configurations. This effect was attributed to the minimization of loop inductances due to the addition of localized capacitances.

Table 12: Coaxial Via Port Configuration

Via Distribution	PKG to PWB port connections
Uniform	1-20
Staggered	1-16
Peripheral	1-12

4.5.5 PDN self-impedance variation with P/G Coaxial TPV Dimensions

The comparison of the PDN profile based on the variation of decoupling via capacitances on the 3D interposer, due to different processes and stack-ups is presented in Figure 72.

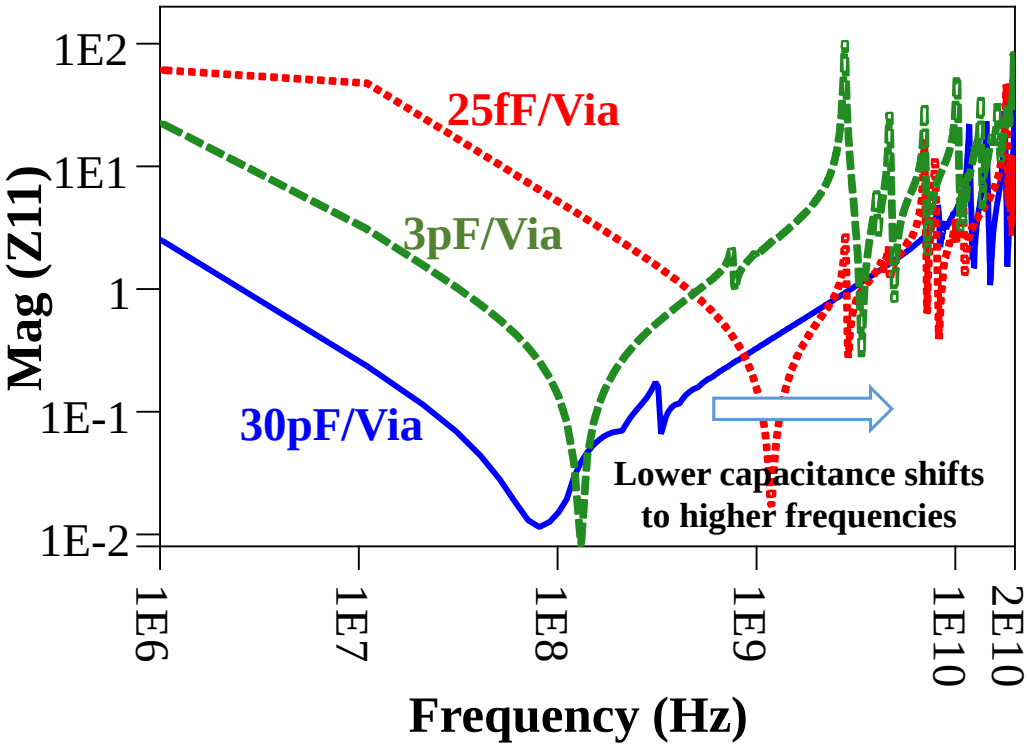


Figure 72: PDN impact due to decoupling via capacitance variation

Three types of via arrangements were considered, - (a) 30pF per via, representing high capacitance density P/G vias in glass (b) 3pF per via, representing P/G capacitances from current generation deposited tantalum oxide films on glass, and (c) 25fF per via, representing polymer based coaxial vias. Each capacitor technology provided decoupling effects at specific frequencies based on their resonance frequencies. The highest PDN benefit was obtained by having the largest capacitance near the die location.

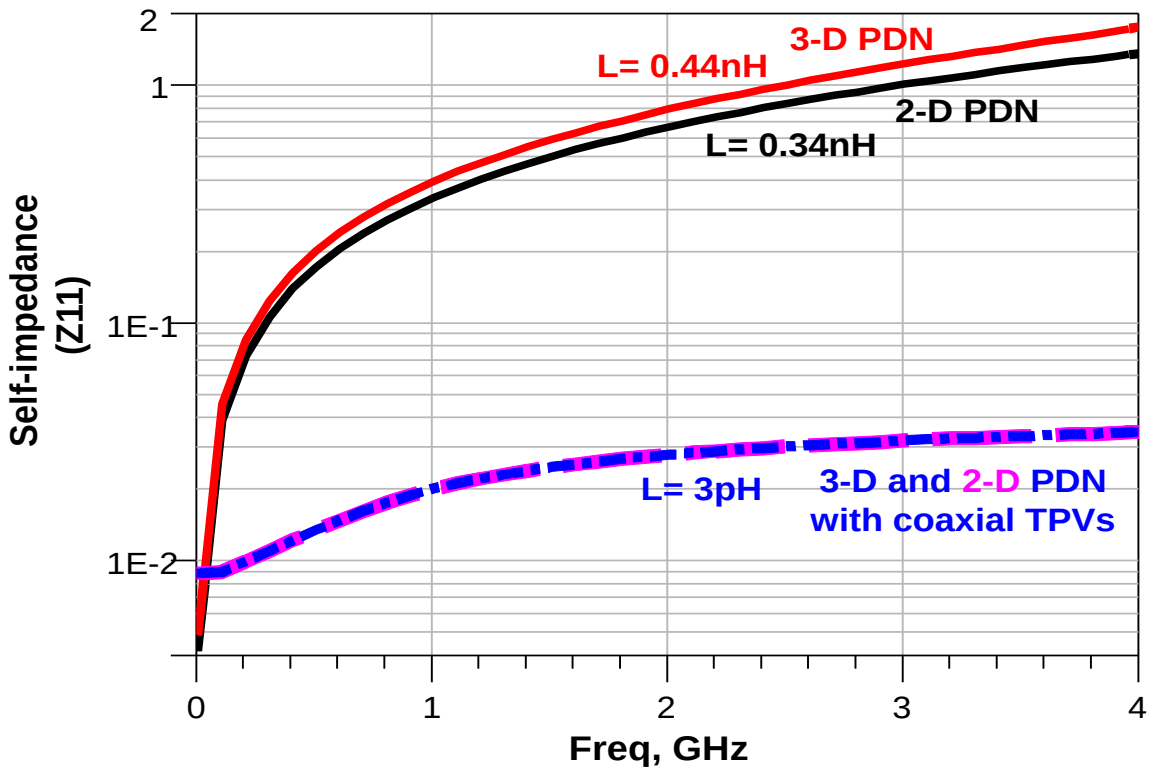


Figure 73: Comparison of PDN inductance and inductance with the addition of coaxial power-ground planes with TPVs

The extracted 2-D and 3-D PDN inductances after the addition of coaxial power-ground with TPVs are plotted as shown in Figure 73. The inductance values of 3-D glass interposers before the addition of coaxial vias were compared based on the simulations from the previous section. The highly-capacitive dielectric liner on the glass substrate completely eliminated the additional inductance of the 3-D configuration, leading to a 100X improvement in PDN impedance. Further, the addition of P/G TPVs completely suppressed the power-ground resonances to meet the target impedance up to 10 GHz. There was no impedance variation in the 3-D configuration when compared to the 2-D PDN due to the removal of BGAs. This effect was attributed to the large distributed capacitance in the P/G plane.

4.5.6 Target Impedance Design with coaxial power-ground with TPVs

The results from coaxial power-ground TPV placement study from the previous sub-sections were used to design the PDN package for a typical logic application. A target impedance of 60 mΩ was used in the PDN design of power-ground plane structure with coaxial TPVs. The targeted frequency range was from DC to till 10 GHz, with a linear increase in target impedance values at higher GHz frequencies, based on the voltage ripple requirements. The placement locations and the cross-section of the coaxial P-G with TPVs on the 3-D interposer package are shown in Figure 74.

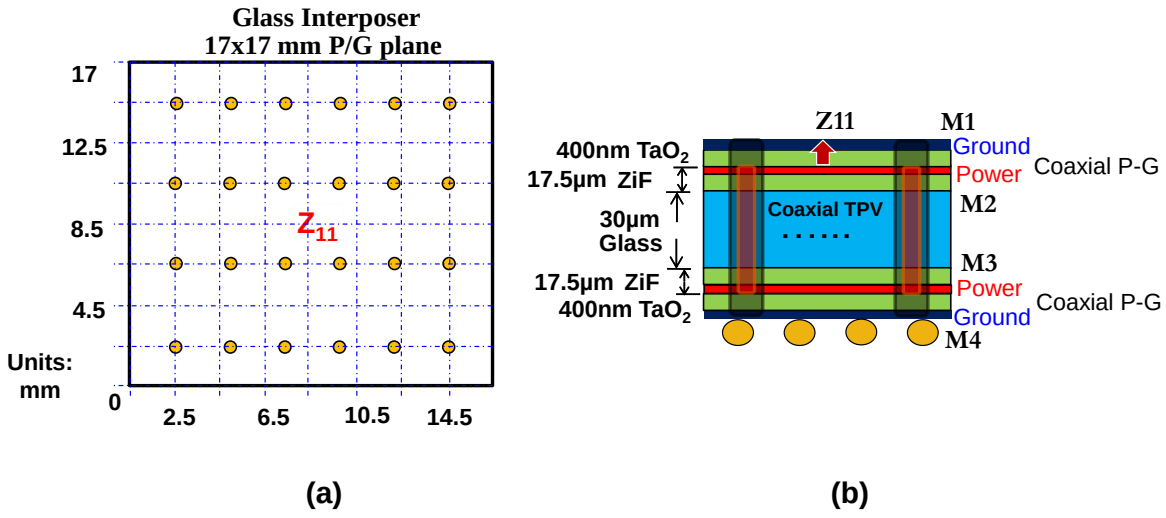


Figure 74: (a) Top View and (b) Cross-section of PDN design using coaxial power-ground with TPVs

The self-impedance of the 3-D PDN system after the placement of coaxial P-G with TPVs is presented in Figure 75. Based on the above analysis, the coaxial power-ground planes and through-vias were demonstrated to reduce the PDN inductance from 440pH to 3pH, resulting in suppression of multiple resonance frequencies between 0.5-10 GHz,

providing an effective and flexible PDN design method for double-sided 3D glass interposer packages.

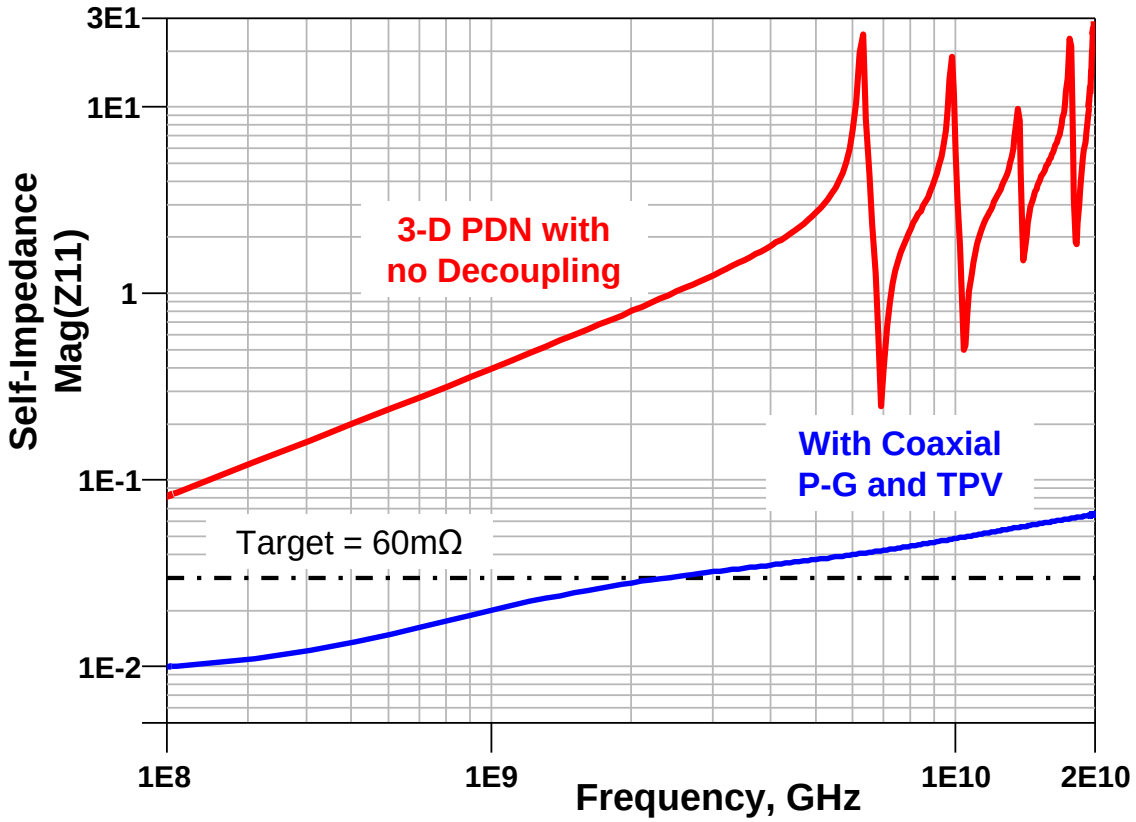


Figure 75: 3-D interposer impedance after coaxial P/G TPV

4.6 Summary of Suppression Solutions for 3-D glass interposers

Resonance suppression solutions were designed based on the critical need to mitigate the magnitude of self-impedance peaks in 3-D glass interposer power delivery networks. The PDN profile of four important design methods introduced in this dissertation were compared in Figure 76 using full-wave electromagnetic simulations. The key findings based on this research are:

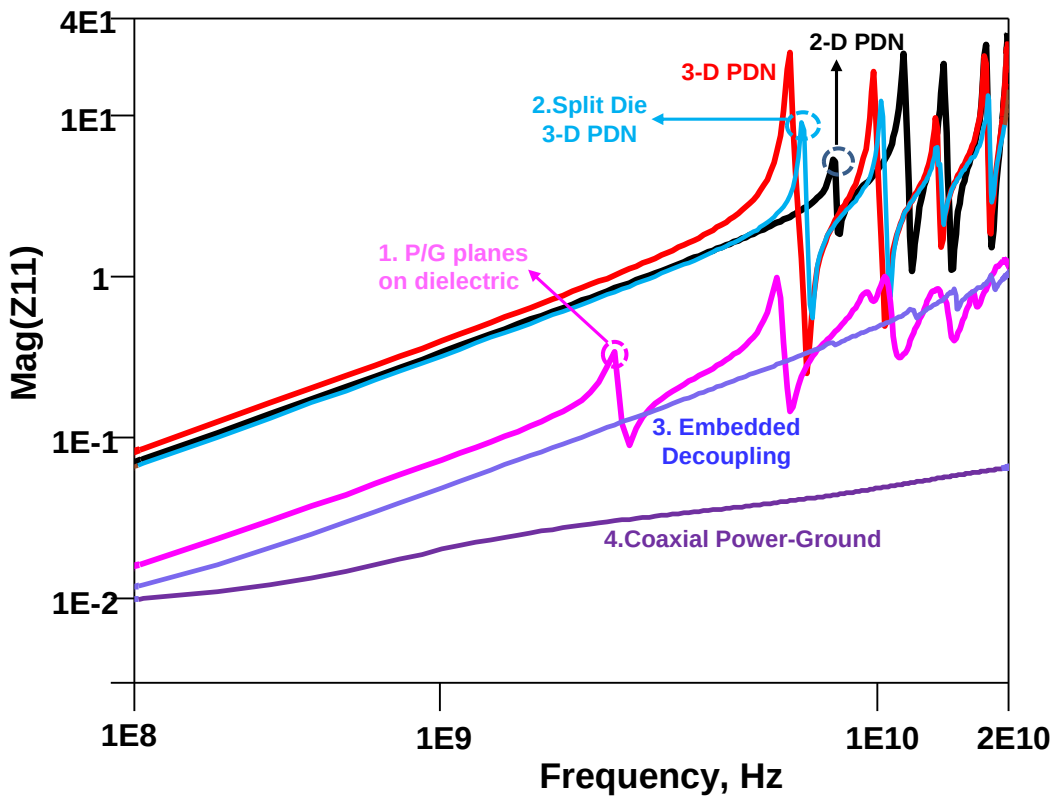


Figure 76: Comparison of 3-D glass interposer resonance suppression techniques

1) Multiple power-ground plane pairs across build-up dielectric

The glass package PDN was designed with two plane pairs across the thin-film build-up dielectric on top and bottom surfaces of the glass core to achieve 10X reduced inductive impedance. The magnitude of the high-impedance peaks were reduced from 180Ω to 0.9Ω at resonance frequencies, providing effective mitigation of P/G resonances up to 4 GHz using this approach in 3-D glass interposer packages.

2) BGA placement in 3-D Glass interposer packages

The PDN impedance profile was analyzed based on variations in the interposer BGA arrangement due to bottom die placement. The lateral trace inductance had a much larger impact on the self-impedance profile when compared to the inductance of parallel

BGA's. Therefore, the magnitude of the resonance suppression using a split die 3-D configuration was much larger (13Ω) than increasing the BGA pitch of the double-sided glass package (31Ω).

3) Embedded Decoupling capacitors within Glass substrates

The selection and placement of embedded decoupling capacitors within the glass substrates was analyzed and compared with discrete SMT-capacitors. The simulations were performed using a signal and power integrity tool – SI-wave. While both embedded and SMT-type capacitors provided resonance suppression at frequencies below 0.1 GHz, the placement of 1nF embedded capacitors decreased the inductive impedance up to 1GHz, to achieve 10X improvement in power integrity at GHz frequencies.

4) Coaxial power-ground planes and vias with high-K liners

The addition of co-axial power and ground planes with TPVs generated a decoupling network between the P/G planes, providing the highest reduction in the magnitude of PDN resonances. A uniform grid distribution of coaxial vias was designed using the results of parasitic extraction and full-wave electromagnetic simulations, to reduce the 3-D package PDN inductance from 440pH to 3pH.

The results from these investigations demonstrate that the ultra-thin 3-D interposer PDN structure was effectively designed to meet target impedance guidelines for high bandwidth applications, providing a compelling alternative to 3-D IC stacking with TSVs.

CHAPTER 5

DEMONSTRATION OF POWER DELIVERY NETWORK AND RESONANCE SUPPRESSION IN 3-D GLASS INTERPOSER PACKAGES

In the previous two chapters, the modeling of 3-D glass interposer PDN to quantify the resonances, and the design of resonance suppression schemes for the high-impedance glass substrate were discussed. This chapter presents the validation of these results by the fabrication and characterization of 3-D glass substrate test vehicles, by integrating through-package-via (TPV) and re-distribution layers (RDL) in ultra-thin glass interposers to form the power delivery network. The first section describes the design and fabrication of 30μm and 100 μm-thick glass substrate test vehicles for electrical characterization. The 3-D glass interposer power delivery network resonances were characterized up to 20 GHz and correlated with the electromagnetic simulation results from Chapter 3. The second section focuses on the measured demonstration of the most important suppression solution for 3-D glass interposers, using decoupling capacitors. The assembly process for the placement of decoupling capacitors on the fabricated glass substrates was studied, based on the design guidelines developed in Chapter 4. The suppression of impedance peaks at the resonant frequencies was verified using a two-port self-impedance measurement technique. The glass samples were also analyzed by micro-sectioning after the placement of SMT decoupling capacitors. The final section presents the electrical characterization of the signal channel with small TPVs in 30μm glass interposers to validate the high BW performance of 3-D glass interposer packages.

5.1 Overview of Multi-layer Glass Interposer Test Vehicles

This section outlines the integration process used to fabricate ultra-thin 3-D glass interposers, ready for double-sided assembly of ICs and assembly to boards. The electrical test vehicles were designed, fabricated, and electrically characterized to demonstrate the feasibility of the approach using power and ground planes in ultra-thin, glass substrates with small TPVs to suppress PDN resonances. Two types of substrates were fabricated to compare the P/G plane self-impedance, namely (a) glass cores of thickness 100µm, having four metal layers, two on each side of the glass core, and (b) ultra-thin glass cores of thickness 30-µm, having two metal layers. The schematic cross-section of the stack-ups used for the test vehicles are presented in Figure 77.

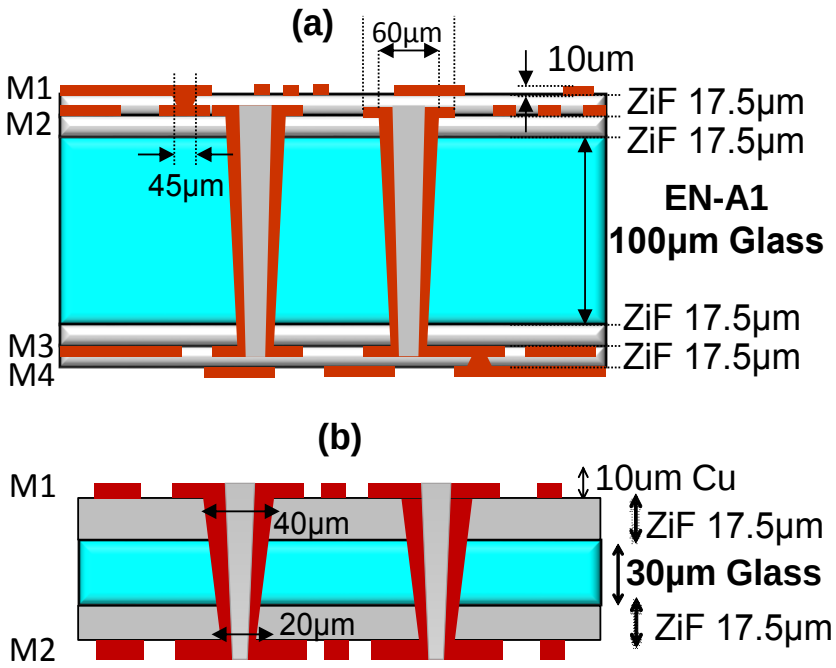


Figure 77: Stack-up of (a) 100µm glass core with four metal layers, and (b) 30µm glass core with two metal layers

5.1.1 Design and Panelization of Multi-layer Glass Interposers

The test vehicle was designed for layout on six inch glass panel substrates (150mm x 150mm square). The PDN self-impedance of 3-D glass interposers were studied with parametric variations in power and ground plane dimensions. The panel-level layout illustrating the designed structures in the test vehicle is shown in Figure 78. The multiple dimensions of the glass packages were used to quantify the impact of varying package body size on the magnitude of power-ground resonances. The four-metal layer test vehicle also included signal transmission line structures with TPV transitions to analyze signal-to-power coupling behavior. In addition to these structures, BGA solder ball structures and SMT decoupling capacitor mounting pads were included to optimize the assembly process as shown in Figure 79 and Figure 80. The metal patterns in the redistribution layers were uniformly distributed using a dummy mesh pattern in order to improve the thickness uniformity of plated copper structures.

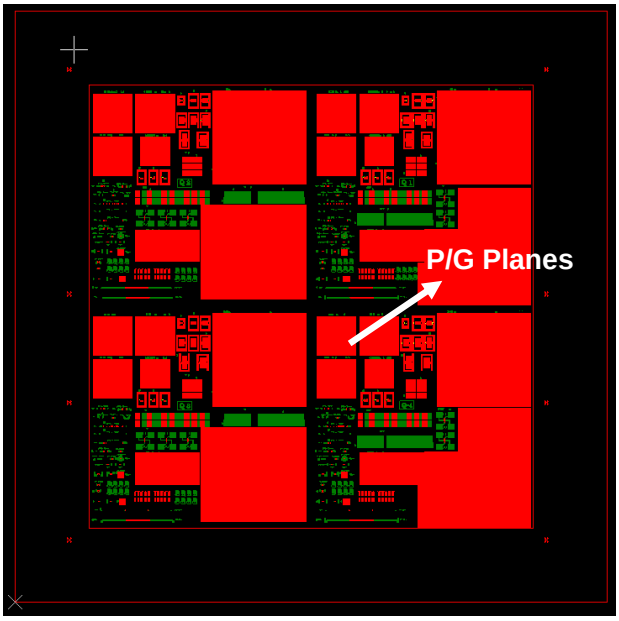


Figure 78: 30µm-thick two-metal layer glass test-vehicle design (150mm x 150mm) showing the layout of the top metal layer

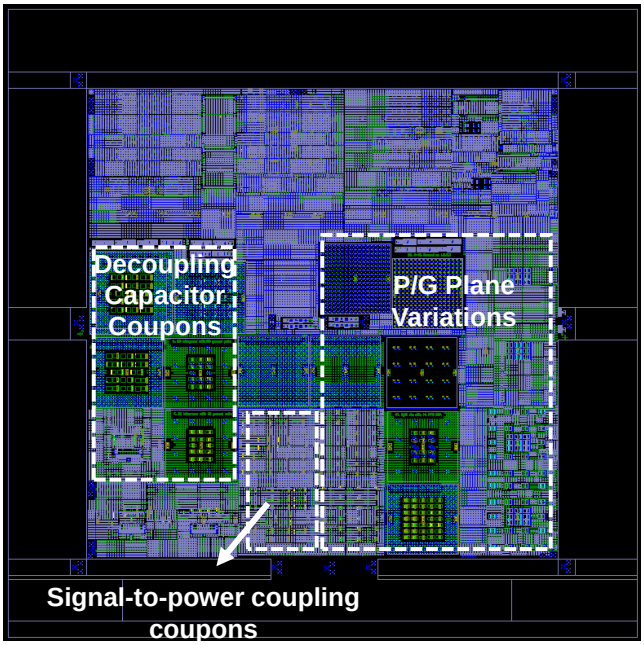


Figure 79: 100µm-thick four-metal layer glass test-vehicle design (150mm x 150mm)

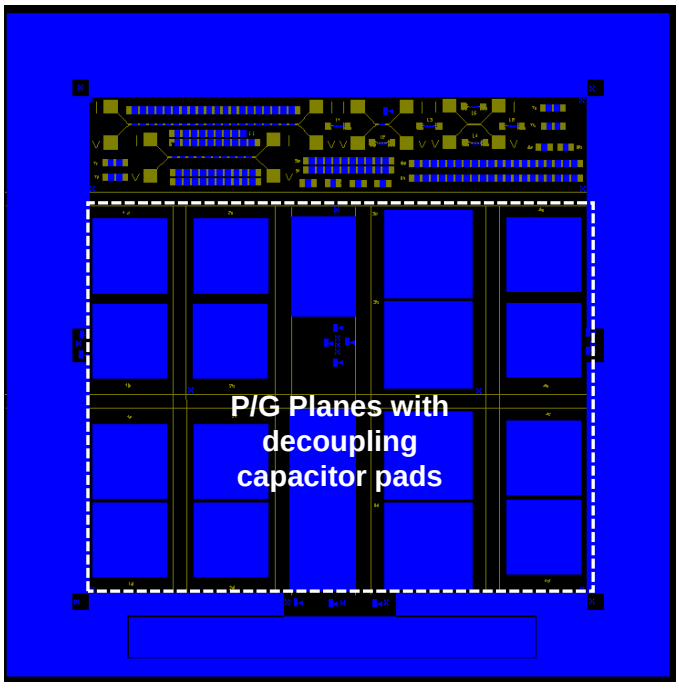


Figure 80: 100µm-thick two-metal layer glass test-vehicle design (150mm x 150mm)

5.1.2 Fabrication overview of Ultra-thin 3-D glass interposers *

This section provides a brief overview of the fabrication process steps for the ultra-thin glass substrates. A panel-based double-side process approach was used for fabricating the test vehicles that were designed in the previous section. The process flow used for the formation and metallization of TPVs was identical for both the four-metal layer and two-metal layer substrates, as illustrated in Figure 81, with additional process steps to form the two build-up layers for the four-metal layer substrates.

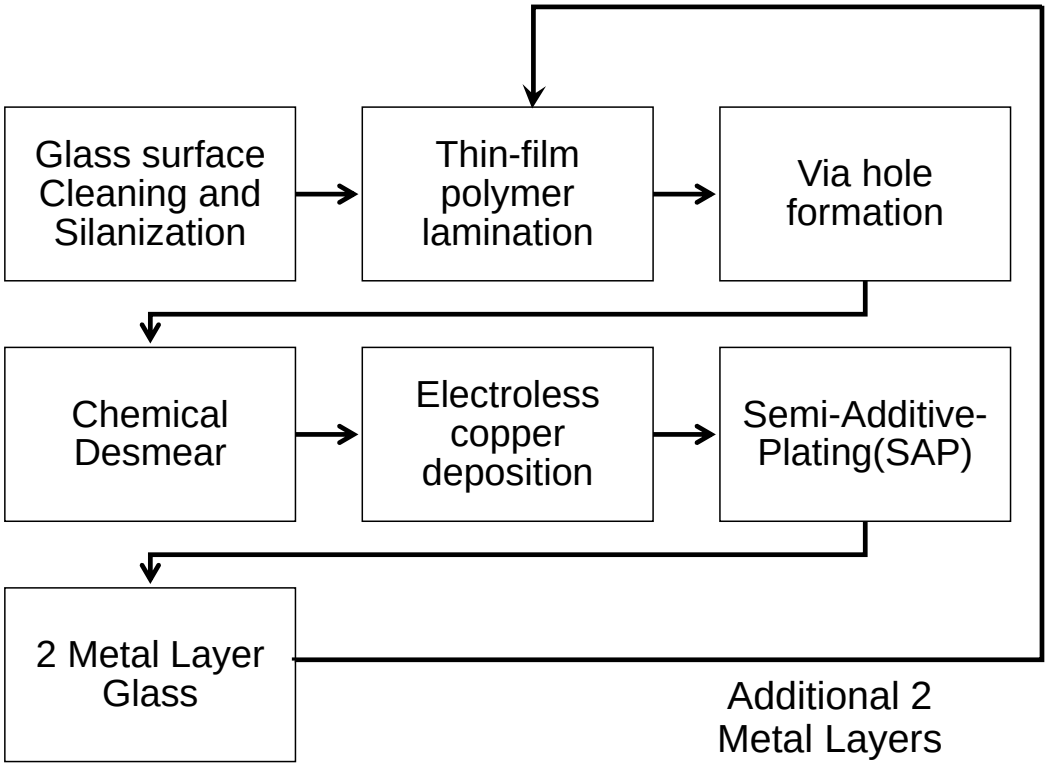


Figure 81: Simplified process flow for multi-layer glass interposer fabrication

* In collaboration with Vijay Sukumaran and Kaya Demir at GT-PRC

A) Glass Surface Cleaning and Silanization:

The glass samples (150mm x 150mm) were cleaned using acetone and isopropyl alcohol (IPA) followed by rinsing with deionized water, to remove any organic contamination on the glass surface due to handling and transport. The samples were then baked for 30 minutes in air at 120°C to remove moisture. Subsequently, the glass surface was treated with silane coupling agents (3-Aminopropyltrimethoxy silane) to promote polymer to glass adhesion through the formation of -Si-O-Si- bonds at the interface.

B) Thin-film polymer lamination:

A 17.5µm thick dry-film polymer (ZEONIF™ ZS-100) was laminated on both sides of the treated glass surface using a vacuum laminator. The key material properties of the dry-film polymer have been reported earlier [29] . The temperature and duration of the lamination process were 120 °C and 90 seconds respectively. The polymer was then cured in an oven at 180°C for 1 hour to ensure complete cross-linking of the polymer chains to achieve the low dielectric constant and low dielectric loss tangent properties of the material. The polymer layer also serves additional functions such as acting as a stress buffer layer and improving the handling of such thin glass panels [58].

C) TPV formation:

The next step in the test vehicle fabrication was the formation of TPVs in the polymer laminated glass substrates. The 30µm thin glass test vehicle design had 40µm diameter TPVs, while the 100µm thin glass test vehicle design had 100µm diameter TPVs. Both these diameters were achieved by UV laser ablation processes that have been previously developed in glass interposers [25] .

D) TPV Metallization and Semi-Additive-Plating (SAP):

After TPV formation, a SAP approach was used to simultaneously metallize the RDL and TPVs with a target copper thickness of 8-10µm. First, a permanganate-based chemical desmear process was used to clean the TPVs and treat the polymer surfaces and the TPV sidewalls for copper seed-layer deposition. Chemical electroless copper plating was used to deposit a thin conductive layer (100-300 nm). A 15µm thin dry-film negative photo-resist (PR) was laminated for imaging the metal patterns using photolithography. Electrolytic plating was used to achieve a final copper thickness of approximately 8-10µm through the photoresist openings. The use of thin-polymer layers on glass helped achieve crack-free handling of glass even at a thickness of 30µm.

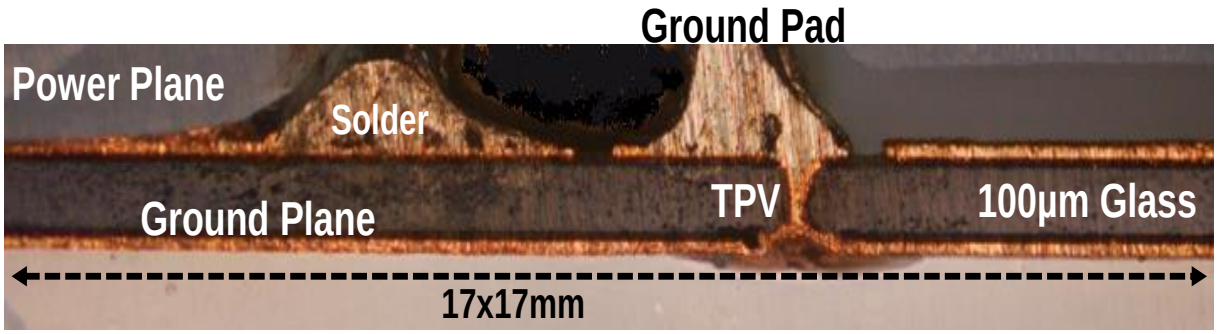


Figure 82: Cross-section of power-ground planes with decoupling capacitor pads in two-metal layer 100 µm electrical test vehicle

A detailed cross-sectional examination was carried out on the fabricated glass samples with TPVs. The power and ground planes fabricated on either side of the polymer-laminated glass core are seen in Figure 83. The via diameter on the entrance and exit side of glass TPVs was observed to be smaller than the openings in the polymer as shown in Figure 82. The difference in via diameters can be attributed to excess ablation during the laser process. [25].

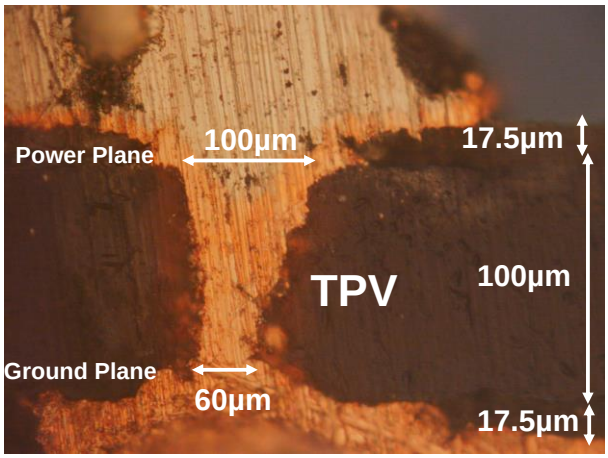


Figure 83: Cross-section detail of TPV in two-metal layer 100µm electrical test vehicle

5.1.3 Measurement Validation of P/G plane resonances in 3-D interposers

This section presents the measured verification of power delivery resonances in 3-D glass interposers. The test vehicles fabricated on 150mmx150mm glass substrates, using panel-based double-side processes [25] described in the previous section, were used to study the PDN impedance profiles of ultra-thin glass interposers. The properties of the glass and polymer materials used in the fabricated samples are summarized in Table 13.

Table 13: Electrical properties of materials used for test vehicle fabrication

Material	Glass EN-A1 (AGC)	Build-up film ZEONIF ZS100 (ZEON)
T_g	720℃	162℃
CTE	3.8 x 10^{-6}	23 x 10^{-6}
Dielectric constant	5.3 at 2.4GHz	3.0 at 10GHz
Dissipation factor	0.004 at 2.4GHz	0.005 at 10GHz

The measurements were performed using a vector network analyzer (VNA) after short-open-load-through (SOLT) calibration. The high frequency characterization of the test vehicles was performed up to 20 GHz with 250μm-pitch ground-signal-ground (GSG) probes, as shown in Figure 84. A two-port self-impedance measurement technique was used to achieve milliohm-scale accuracy as presented in Figure 85 [89].

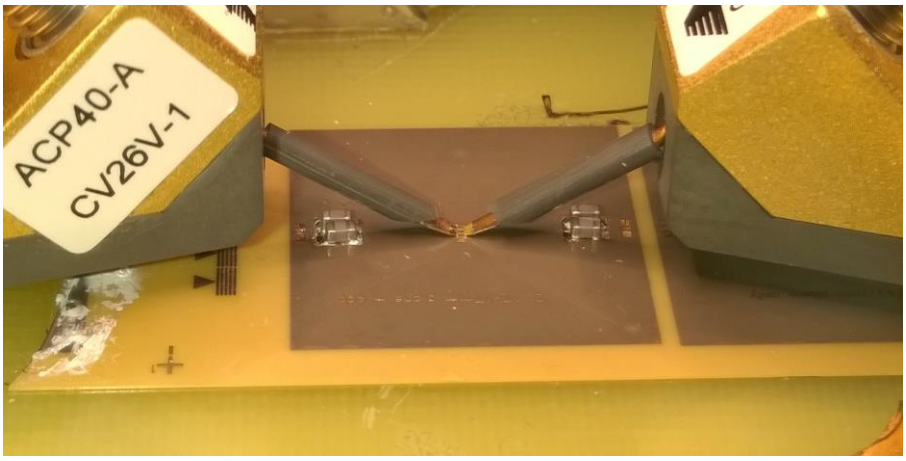


Figure 84: VNA measurement arrangement of glass interposers

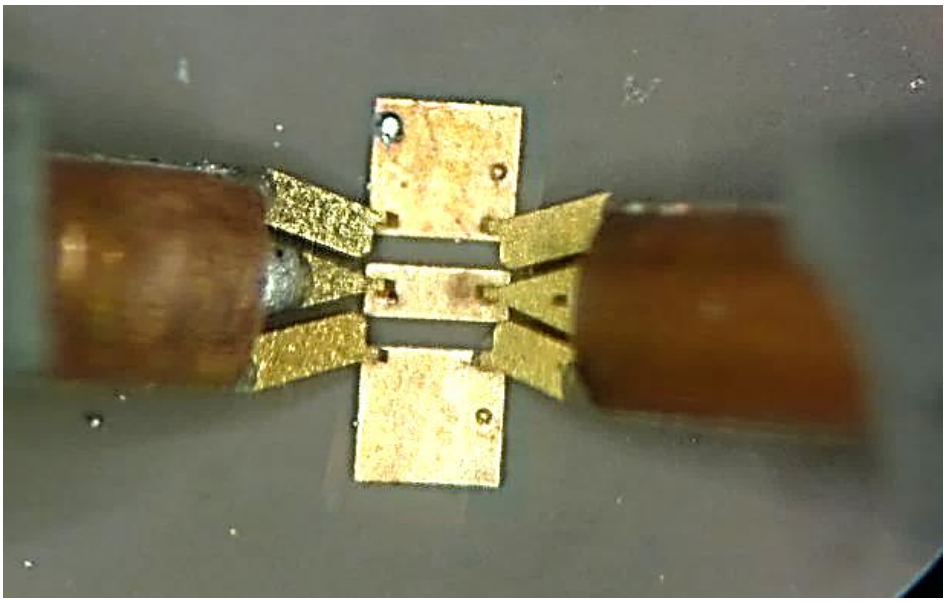


Figure 85: Probe arrangement for PDN Measurement of 3-D glass interposers

Various interposer dimensions were designed and characterized with parametric variations in power-ground plane size from 10mm x10 mm to 25mm x 25mm. The details of the individual P/G plane coupons and port locations are presented in Figure 86.

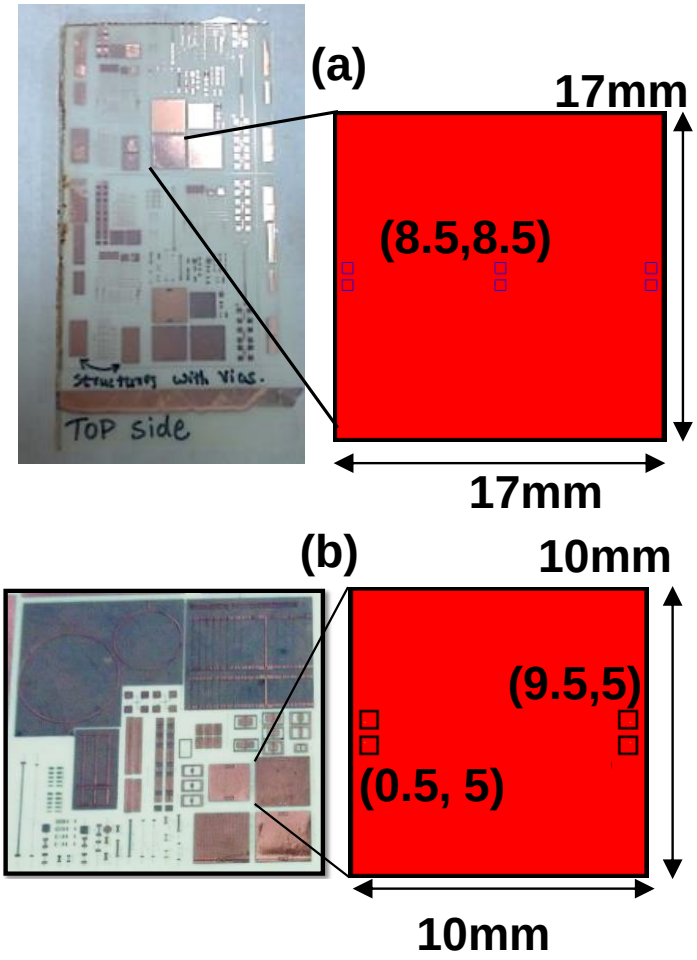


Figure 86: Top view of (a) 100µm and (b) 30µm glass test vehicles showing port locations

A) Measurement of power-ground plane resonances of 100µm-thick glass substrates:

The self-impedance (Z11) measured at the center of the 17mmx17mm P/G planes across the 100µm-thick glass is plotted in Figure 87. The sample was probed on the top metal layer (M1) using pads connected to the planes through blind microvias and TPVs,

as shown in Figure 86 (a). The measured mode resonances were in agreement with the simulation results. The shift in the first series resonance of the measured impedance can be attributed to variation of the metal thickness and consequently that of the dielectric layers during fabrication. Overall, there was good correlation between the simulated and measured responses. The magnitude of the mode-resonant peaks in the measured results was suppressed due to the contact resistance of the probe pads.

Table 14: Measurement comparison of P/G resonances for 17mm x 17mm glass interposers

Calculated (GHz)	Measured (GHz)	M	N
8	8.01	2	0
11.05	11.7	2	2

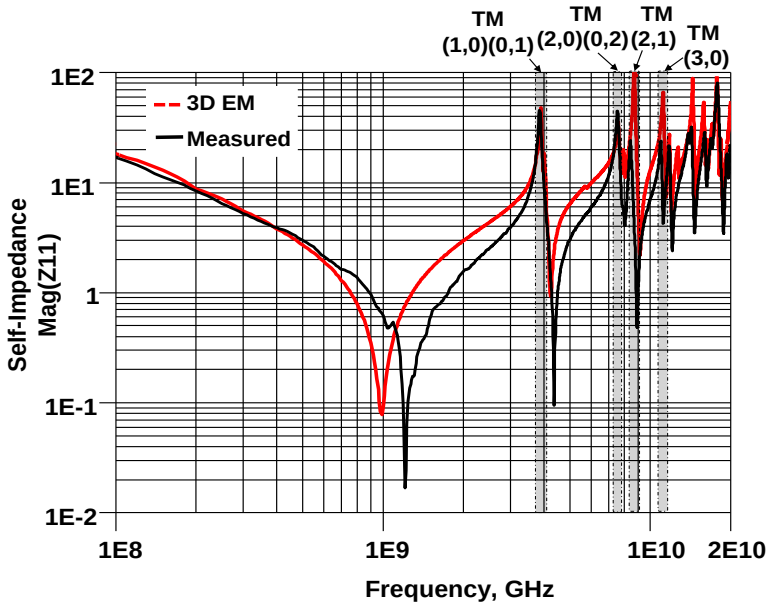


Figure 87: Measured self-impedance (Z11) for 17mmx17mm P/G planes across 100µm-thick glass

B) Measurement of power-ground plane resonances of 30µm-thick glass substrates:

P/G planes of dimensions 10mm x 10mm were fabricated using ultra-thin glass having a thickness of 30µm to demonstrate the effects of change in interposer stack-up on the PDN self-impedance.

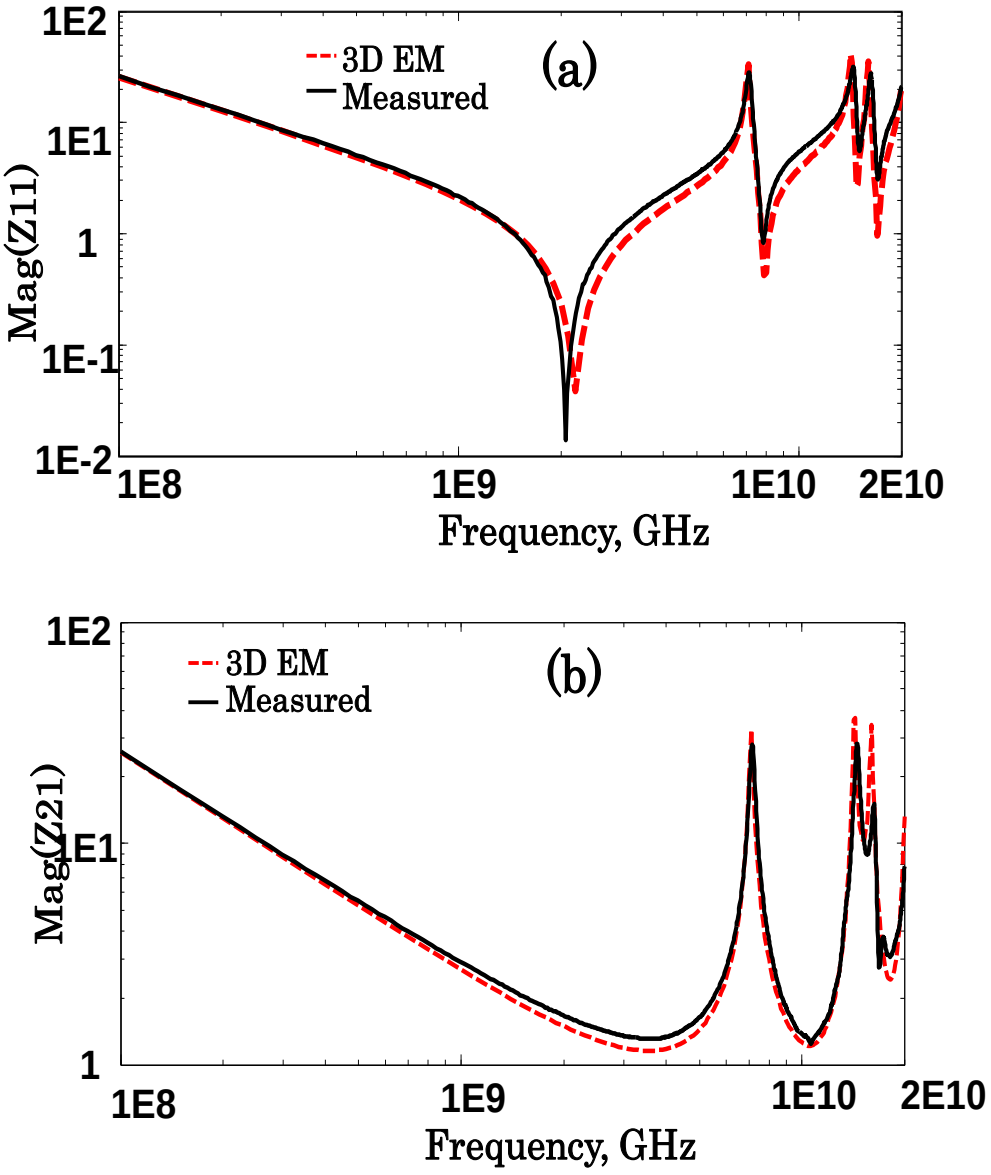


Figure 88: Measured (a) self (Z11) and (b) transfer (Z21) impedance for 10mmx10mm P/G planes across 30µm-thick glass

The self-impedance and transfer impedance (Z21) were measured at ports located near the edge of the P/G planes (shown in in Figure 86b), and used to analyze the overall plane impedance. These results are plotted in Figure 88, showing excellent correlation between the measured and simulated responses for both plots. The capacitance and inductance of the PDN were lower owing to the smaller size of the planes, leading to a shift of the mode-resonances to higher frequencies. The improved suppression in this case occurs due to the thickness reduction between the power and ground layers, when compared to the previous 100µm-thick glass.

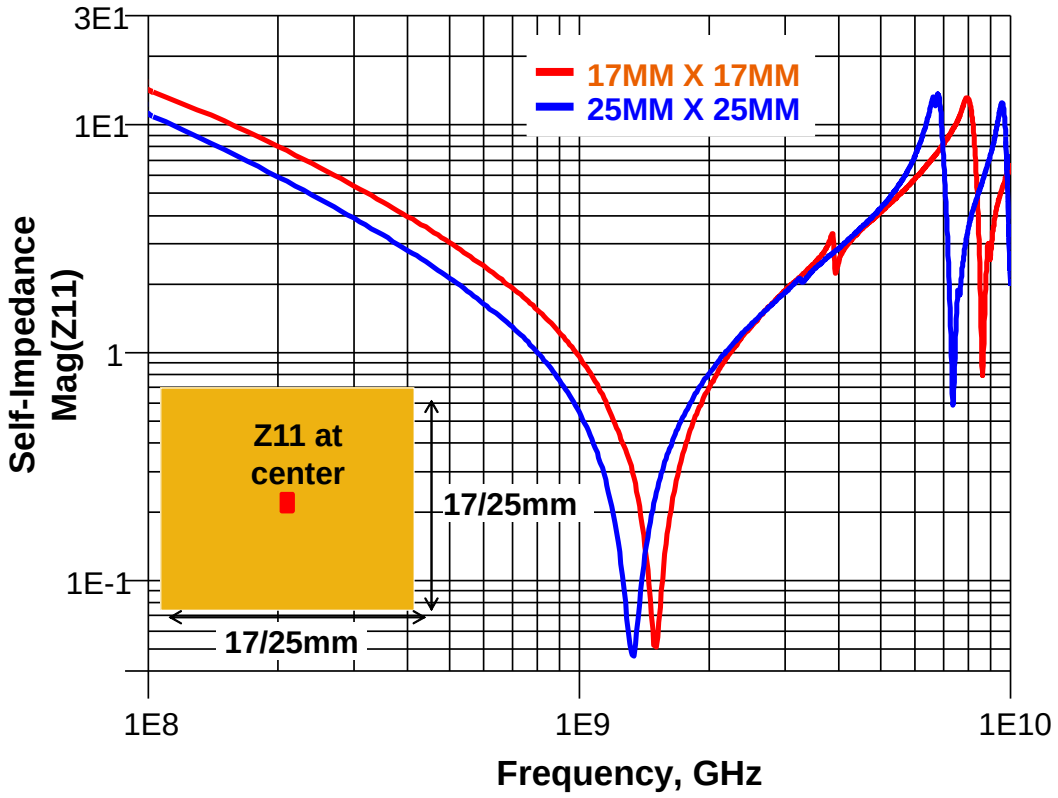


Figure 89: Comparison of measured self-impedance (Z11) for P/G planes of different sizes across 100µm-thick glass

C) **Power-Ground resonances due to interposer size variations:**

The effect of size variation in glass substrates was examined by comparing the self-impedance of multiple P/G plane pair sizes. Parametric variations of interposer sizes 7-25mm^2 were performed on both the 100µm and 30µm stack-up configurations as presented in Figure 89, and Figure 90 respectively. In addition, the port impedance was measured at both the center and edge locations as illustrated in each figure in order to understand the self-impedance with spatial variations. As an example, the measured self-impedance of two different substrate sizes in the 30µm glass with the ports located near 0.5mm inside the central edge is shown in Figure 90.

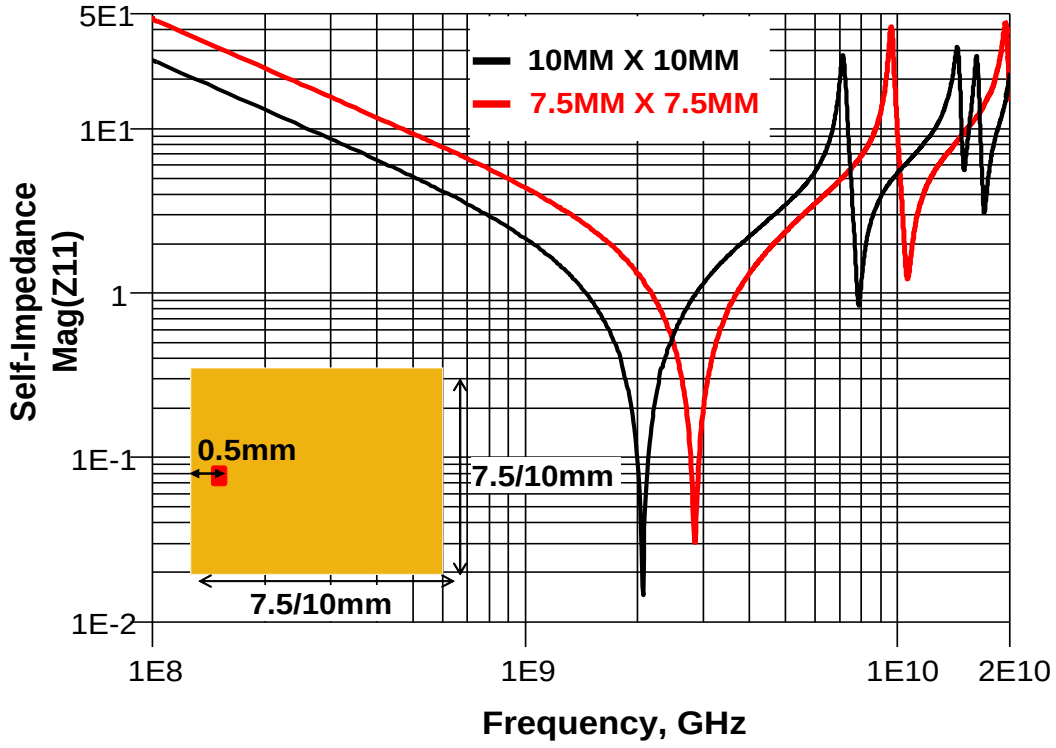


Figure 90: Comparison of measured self-impedance (Z11) for P/G planes of different sizes across 30µm glass

The smaller interposer size (7.5mmx7.5mm) was compared with the 10mmx10mm interposer analyzed in the previous sub-section. The smaller size interposer resonated at a much higher frequency than the larger size interposer, due to the change in resonance cavity dimensions. However, there was a reduction in the total plane capacitance with smaller size P/G planes, similar to the observation in the previous example, leading to higher impedance of the overall PDN network. A similar trend was observed in case of the 100µm glass as illustrated in Figure 89.

5.1.4 Measurement Validation and Characterization of 2-D and 3-D PDN self-impedance in glass interposers

Test coupons having BGA pads on the M4 metal layer were designed in 100 µm-thick glass substrates, to compare the self-impedance of 2-D and 3-D glass package PDN. In both cases, the 17mm x 17mm planes were modified to have an aray of BGA pads at a pitch of 500 µm. The top view of the 2-D and 3-D PDN P/G plane coupons and BGA locations are shown in Figure 91. The 2-D interposer was designed with a BGA array having a total of 730 P/G BGAs. Of these, 170 P/G BGAs located at the center of the interposer provided a direct PDN path to the PWB. These P/G BGA pads located within the 10mmx10mm area were removed to represent the 3-D interposer PDN schematic, resulting in 560 P/G BGA connections. In order to isolate the parasitics of the 3-D glass interposers without the effects of the PWB components, and to extract the effective impedance as seen from on-chip PDN, all the BGA pads were shorted using sputtered copper having a thickness of 1-3 µm.

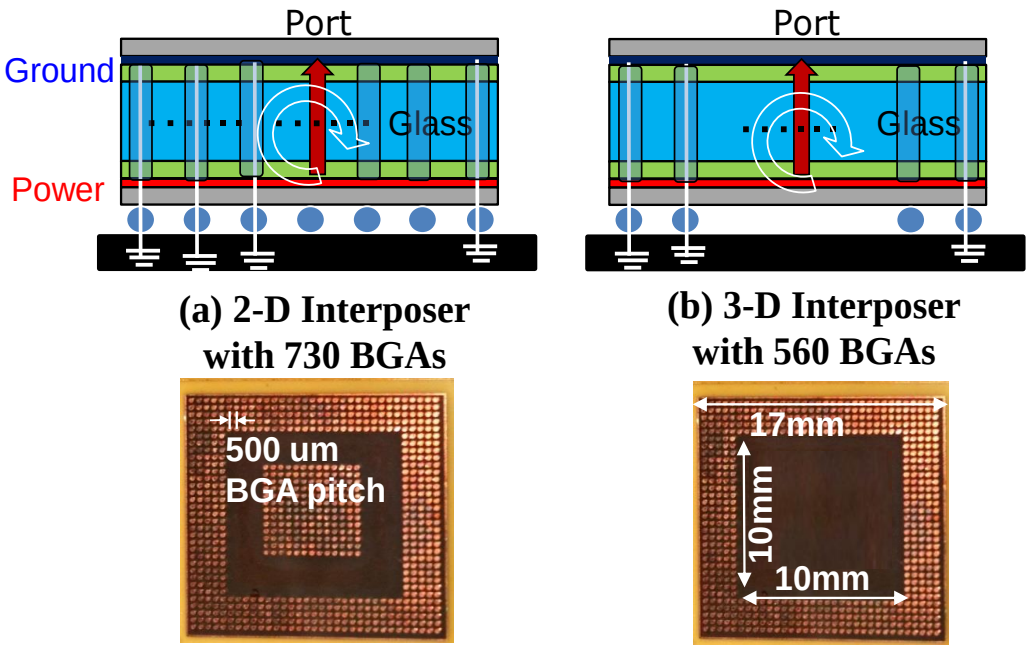


Figure 91: (a) 2-D and (b) 3-D interposer PDN design with bottom view

The characterization for both PDN scenarios is presented in Figure 92. The 3-D interposer PDN exhibited an overall increase in inductive impedance when compared to the 2-D scenario due to the lateral inductive path. In addition, a new high-impedance peak occurred at 7.4 GHz, which correlates well with the 3-D PDN simulation results. This impedance peak was not prominent in the 2-D PDN configuration due to reduced inductance arising from the presence of central P/G interconnections exactly under the center (on-chip) probing location on the other side of the substrate. The high-impedance peaks in the 3-D PDN were not observed at frequencies below 7 GHz due to the small value of the lateral trace inductances. Hence, 3-D PDN structures can meet the target impedance profile for core-PDN design without significant impact, due to negligible current requirement at GHz frequencies.

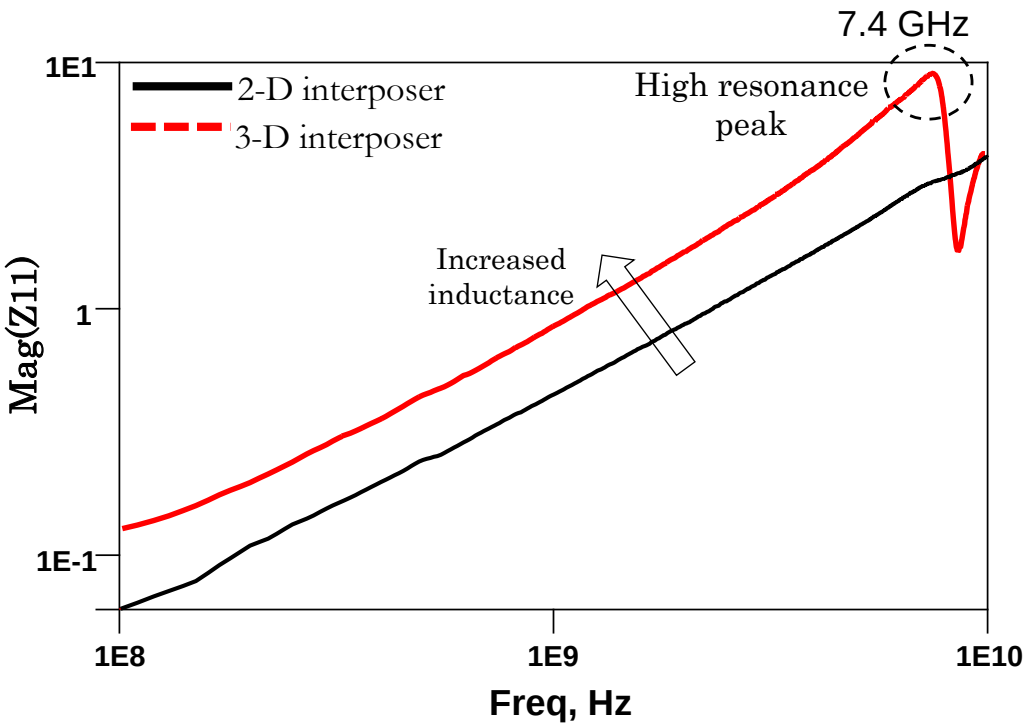


Figure 92: Measured PDN Self-Impedance of (a) 2-D glass package and (b) 3-D glass interposer package

5.2 Measurement Validation of Resonance Suppression with Decoupling Capacitors

This section describes the demonstration of the suppression of power-ground resonances in glass interposers using SMT decoupling capacitors, based on the placement and optimization studies discussed in Chapter 4. A cross-section schematic of an SMT decoupling capacitor placed on the top layer of the 100 μm-thick glass, including the power-ground planes with solder connections and TPVs is shown in Figure 93.

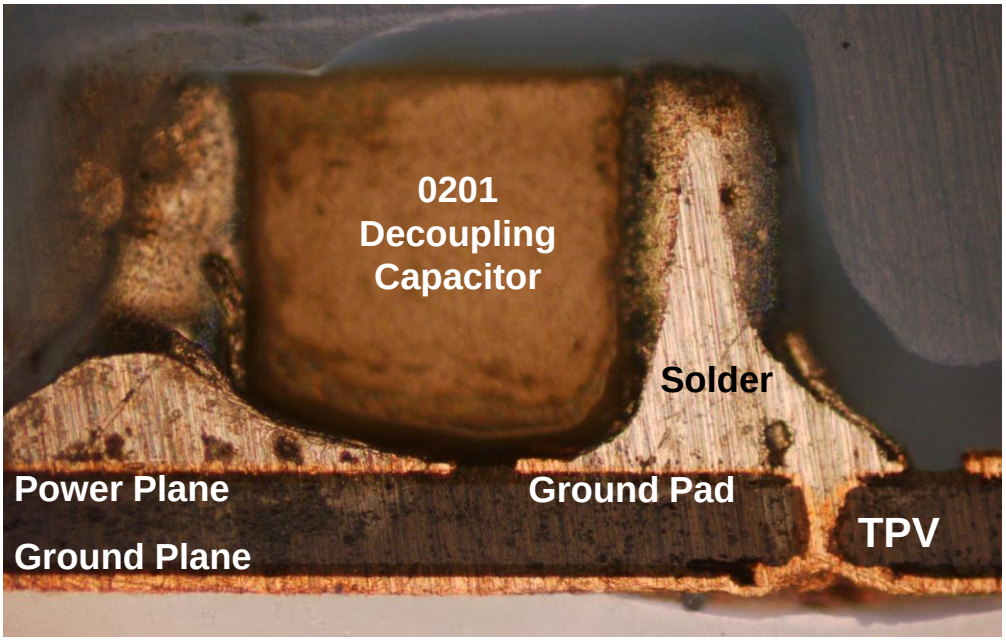


Figure 93: Optical image of cross-section of decoupling capacitor placed on 3-D glass substrate with TPVs and two metal layers

Prior to assembly, the copper surface was cleaned with nitric acid to remove the native oxide surface and provide a clean and oxide-free surface required for solder wettability. The solder paste used was a SAC 305 alloy with a melting point of 217 ºC. The solder particle size was conditioned according to Class 5 paste. The paste was deposited on bare copper (clean) to maximize surface coverage. This method prevented the exposure of copper to air during the assembly process. A no-clean liquid flux material from Alpha NR-200 was used, which is compatible with lead-free applications. The fluxing action enabled the solder material to melt locally and provide good wettability in order to achieve a thin tin layer required for SMT assembly. The reflow profile was modified to include a plateau at 110 ºC for 30s for flux activation. The capacitor was placed such that the electrodes on both sides are in contact with solder on the individual pads. During reflow, the solder wets the electrodes and forms the joints in the shape as

shown in the cross-section in Figure 93. The solder was also confined to the desired area due to the oxidation of copper. Before the placement of SMT-capacitors, a pre-reflow of solder was performed to avoid solder bridging action. This step avoided the spread of the solder paste during the viscous phase, which can result in bridging between the pads during the placement of small components.

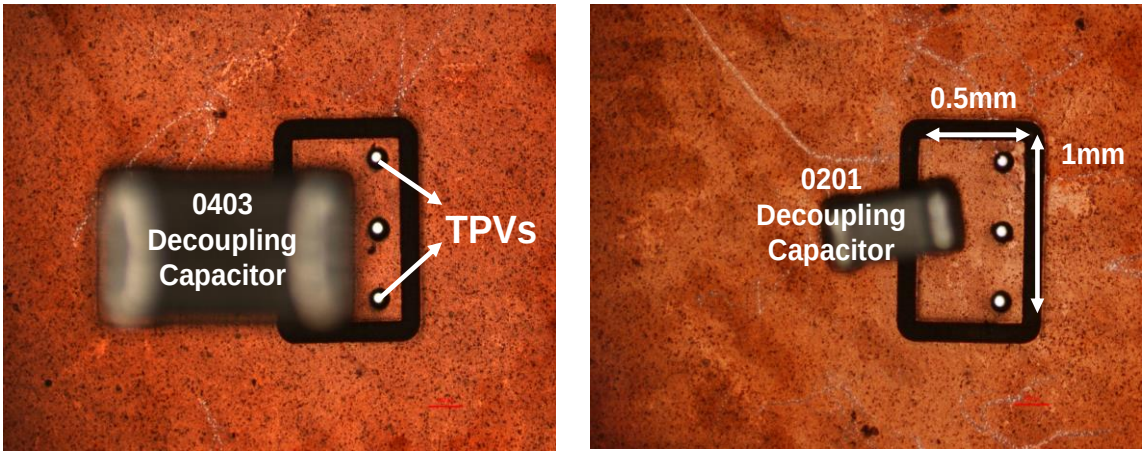


Figure 94: Top view comparison of SMT-decoupling capacitor sizes for glass interposer applications

The reflow profile was built to match the recommended reflow conditions from the paste maker, with a peak temperature of 260C and a dwell time of 15s at peak temperature. The reflow was performed using a Finetech Lambda flip-chip bonder. The bonding process was performed in air to increase processability. The use of reflow oven may also result in the placement inaccuracy of small devices due to nitrogen circulation, after the flux evaporation. This reflow was a soak profile with 4 phases: pre-heat, pre-reflow, reflow and cooling. The assembly of decoupling capacitors on glass interposers was repeated for multiple values and sizes of SMT components. The placement of SMT

decoupling capacitors of various sizes (0201 and 0403) on bond pads located on the top metal layer is shown in Figure 94. Multiple TPVs were connected to one component landing pad in order to reduce the ESL-loop inductance. The smaller size decoupling capacitors were studied due to their ability to provide higher frequency decoupling with lower overall ESL values. A small amount of solder was deposited on the bond pad and reflowed prior to the placement of the component to enable accurate manual placement of components.

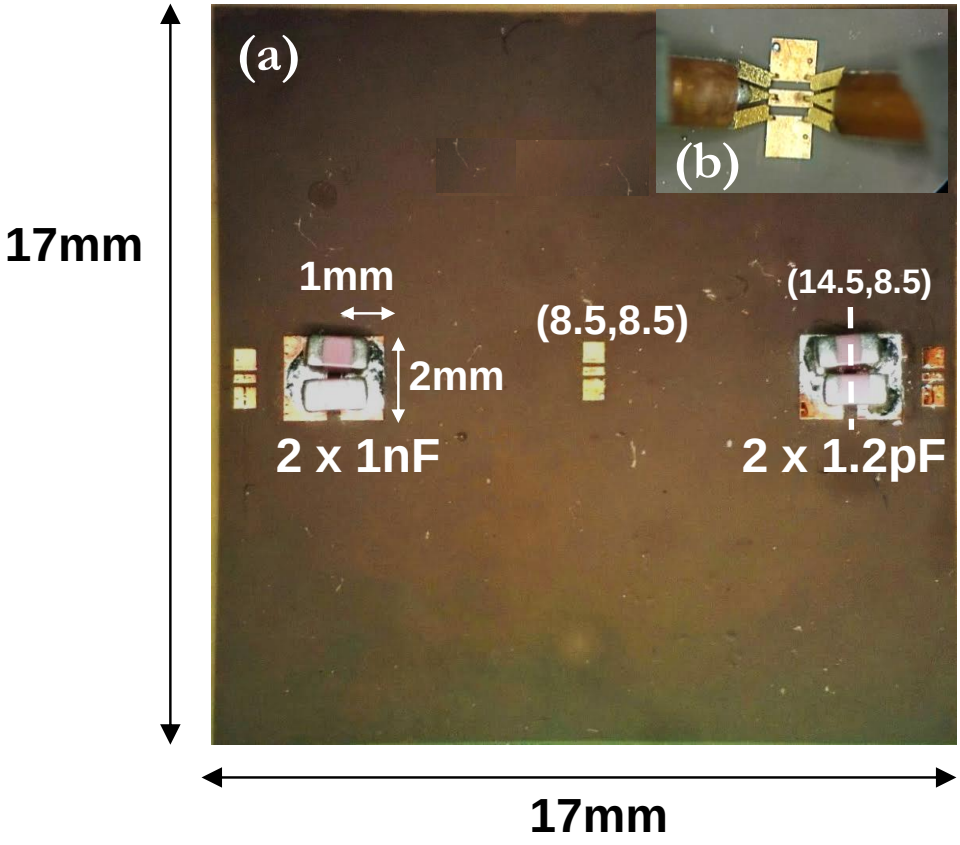


Figure 95 : Decoupling capacitor placement on P/G planes (a) Top view and (b) probe arrangement

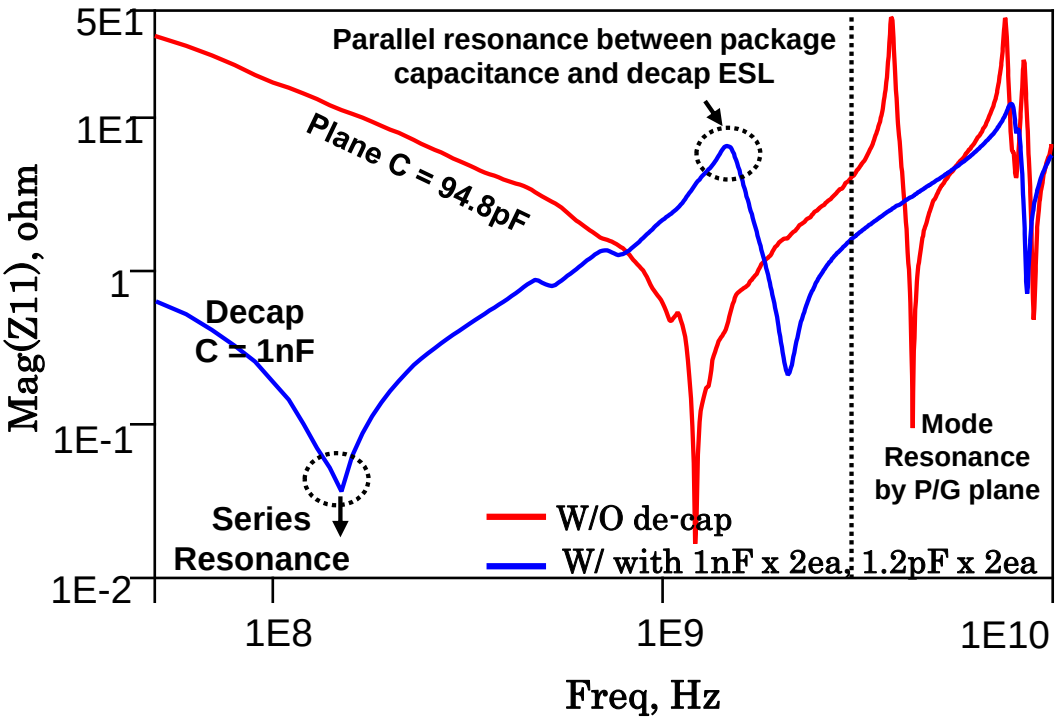


Figure 96: Measured self-impedance (Z11) comparison of 17x17mm^2 P/G planes with 0603 decoupling capacitors

To verify the impact of decoupling capacitors on resonance suppression, four different SMT decoupling capacitors (2x1nF and 2x1.2pF) were mounted on the top layer of the 100μm thick glass substrate. Two capacitors were mounted on each pad to reduce the ESR, and were connected to P/G planes using TPVs. The measurement was performed at the center of the plane, with the capacitor SMT pads located 2.5mm away from the edge of the planes as shown in Figure 95. This location was chosen in order to represent a 3-D PDN configuration with a bottom mounted die, which restricts the placement of the land side capacitors near the center of the interposer. The self-impedance with and without decoupling capacitors is compared in Figure 96. The capacitors were effective in decoupling at frequencies below 1 GHz. However, at 1.4 GHz, a new high-impedance

peak was created due to the parallel resonance between the package P/G plane capacitance and the combined ESL of the capacitors, mounting pads, blind vias and TPVs. The 1.2pF capacitors did not suppress high frequency resonances due to the ESL and the large trace length between the point of mounting and the center probe. Thus, SMT discrete decoupling capacitors were not effective in reducing the inductive impedance at GHz frequencies, where additional high-impedance peaks are generated in 3-D interposers. Therefore, the placement of decoupling capacitors must be carefully considered for 3-D glass interposer designs.

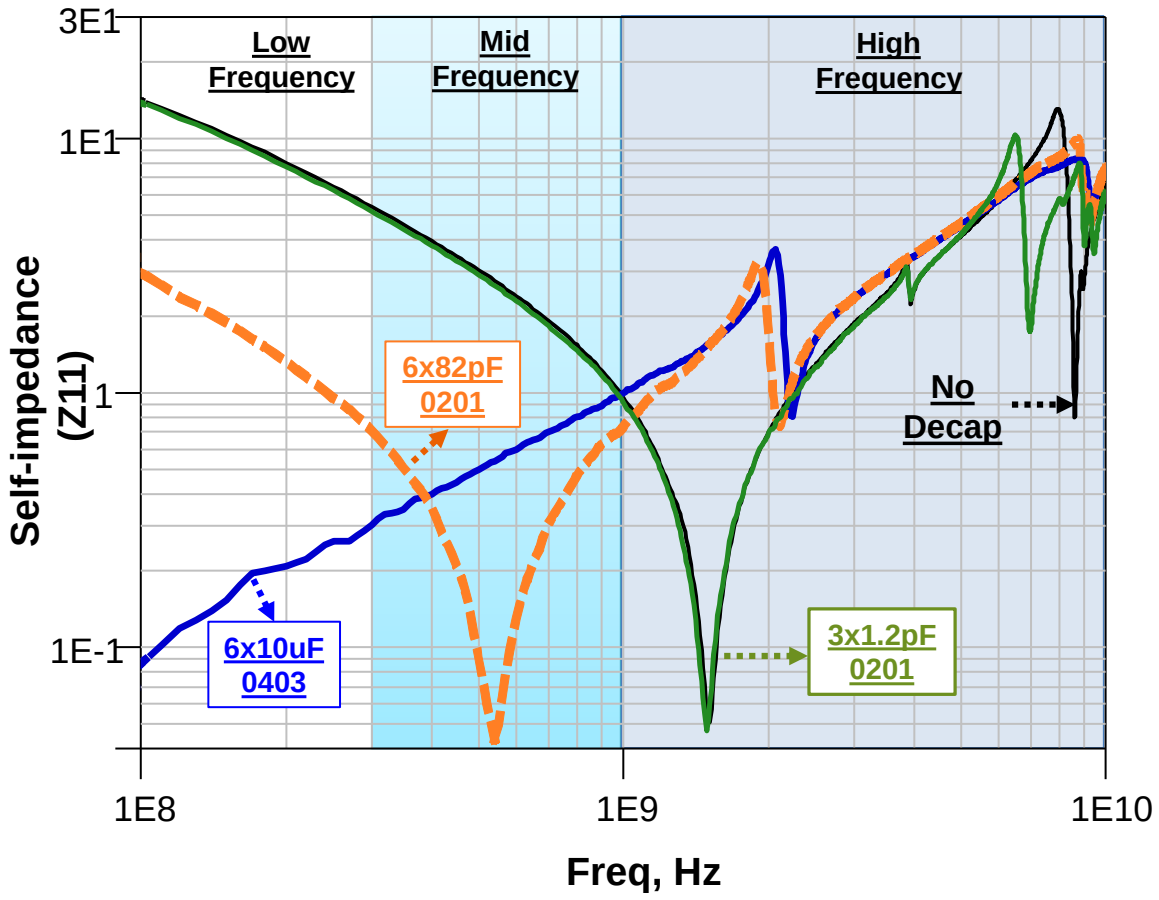


Figure 97: Measured self-impedance (Z11) comparison of 17x17mm^2 P/G planes with decoupling capacitors at low, mid and high frequencies

Based on this analysis, the comparison of resonance suppression at three different frequency regions was examined with multiple values of decoupling capacitors, as seen in Figure 97. The size of the glass interposer was chosen to be 17x17mm^2 for this study. Three values of capacitors (10uF, 82pF, and 1.2pF) were selected to provide decoupling at low, mid and high frequencies respectively. The capacitors were distributed uniformly on the top power layer of the glass interposer. The measured self-impedance results proved that the PDN resonances in 3-D glass interposers were effectively suppressed with the appropriate decoupling capacitor network design, similar to organic packages.

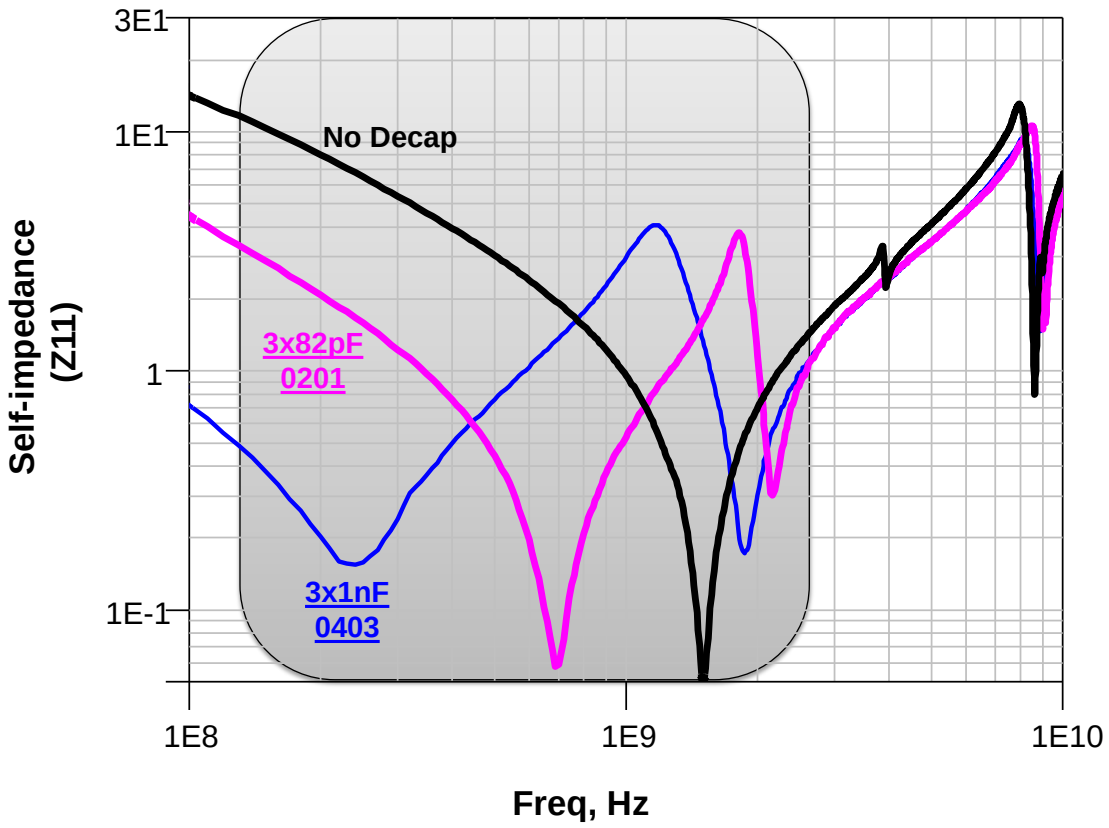


Figure 98: Measured self-impedance (Z11) comparison of 17x17mm^2 P/G planes with decoupling capacitors for mid-frequency suppression

The suppression of mid-frequency impedance was examined, as seen in Figure 98, using both 1nF and 82pF decoupling capacitors. Three capacitors of both values were mounted on the ground plane at the bottom of the glass interposer. The measurement was performed at the center of the power and ground planes. The results indicated that such decoupling networks provide approximately 10X reduction in the inductive impedance at mid-frequencies below 700 MHz.

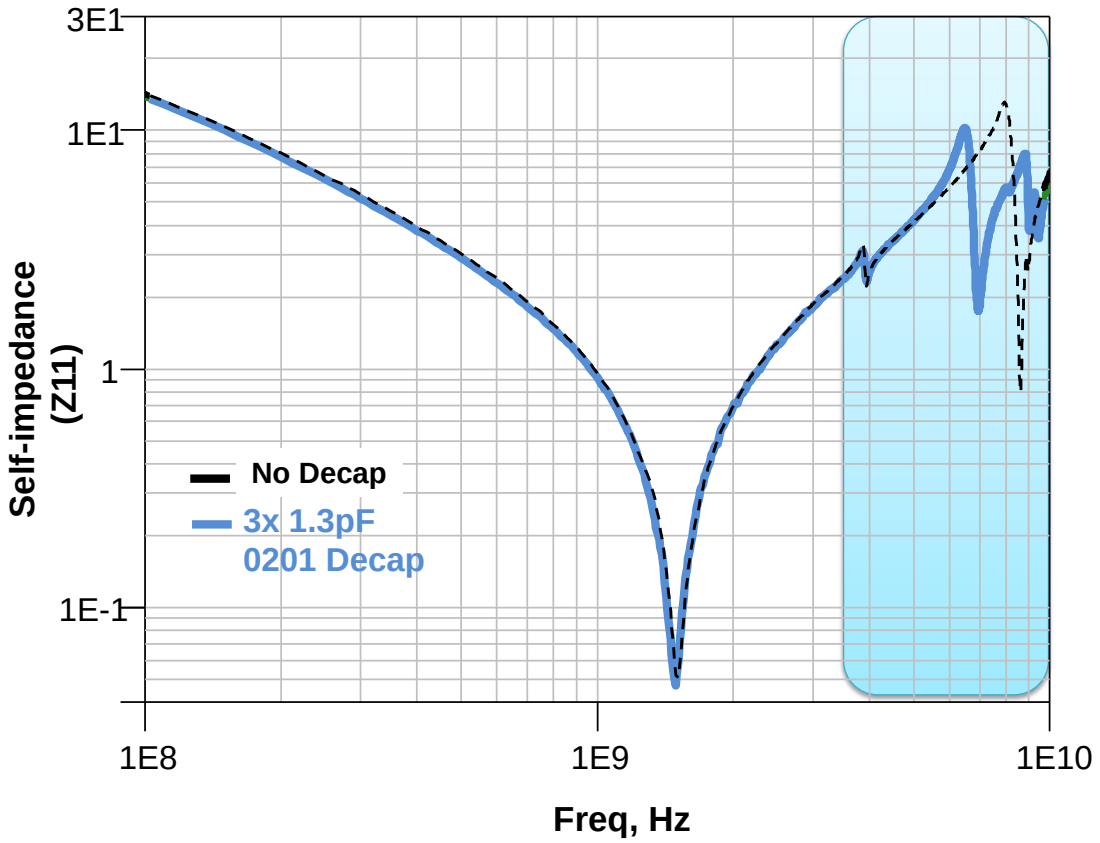


Figure 99: Measured self-impedance (Z11) comparison of 17x17mm2 P/G planes with decoupling capacitors for high-frequency suppression

The study was extended to evaluate the effect of placement of decoupling capacitors at GHz frequencies in Figure 99. Three low-ESL 1.3pF capacitors were placed on the ground plane below the probe location. Measured verification of high frequency resonance suppression at 7 GHz was demonstrated after the placement of the decoupling capacitors. However, the small capacitance values were not sufficient to mitigate the magnitude of the PDN impedance. Additional parallel-resonances were also generated at 5 GHz attributable to the ESL interactions of the decoupling capacitors with the power and ground plane capacitance.

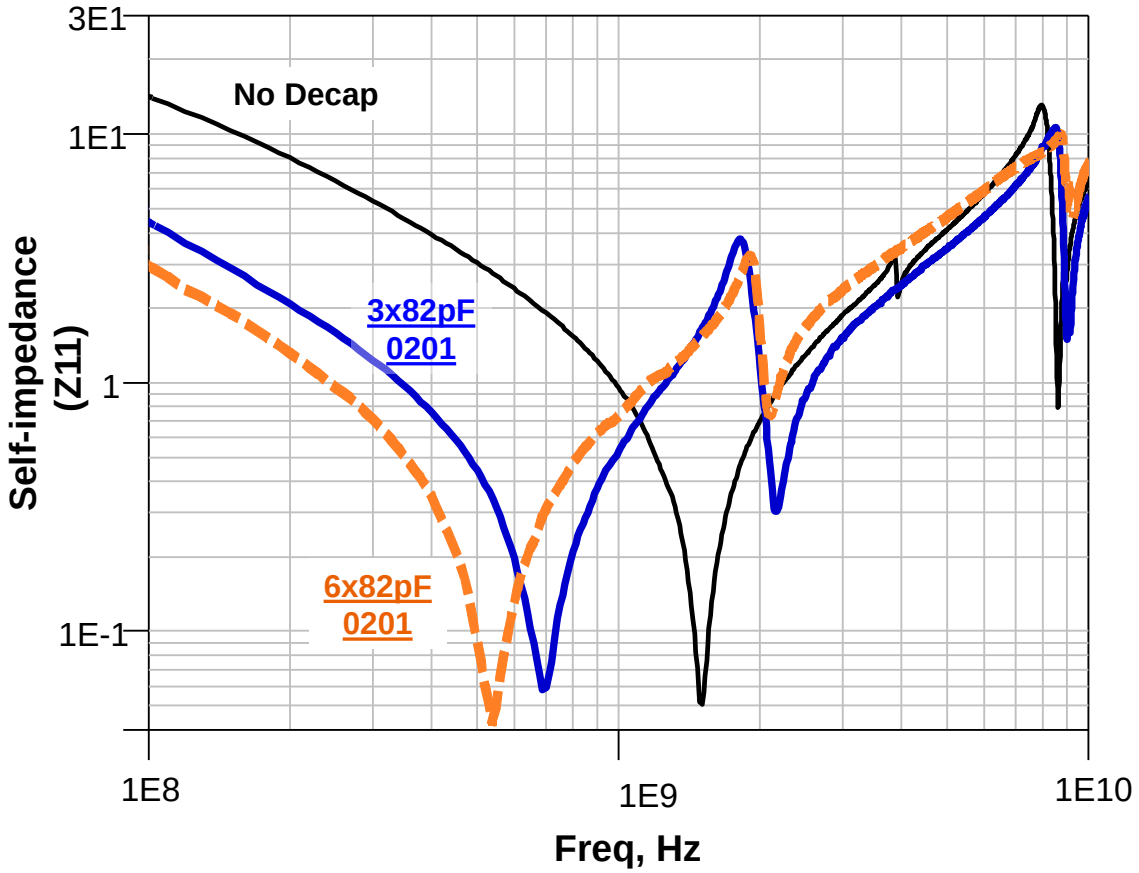


Figure 100: Measured self-impedance (Z11) comparison of 17x17mm^2 P/G planes with variations in number of decoupling capacitors

The suppression impact due to the number of capacitors was studied as shown in Figure 100. The 82pF capacitors analyzed in the previous sub-section were used in this investigation. The measured self-impedance results verified the reduction in the magnitude of the PDN network resonances with the addition of decoupling capacitors. This effect was attributed to the addition of parallel capacitors, which reduced the inductance and resistive impedance of the glass interposer. Based on the measured self-impedance results presented in this section, it can be concluded that the design of the decoupling capacitive network serves as an effective PDN noise suppression solution in 3-D glass interposer packages.

5.3 Demonstration of High BW signal channel with 30 µm ultra-thin glass interposers

Following the demonstration of effective PDN network performance and resonance suppression solutions in 3D glass interposers, electrical characterization of the signal lines in the two-metal layer ultra-thin glass interposers was carried out in [25] to demonstrate the high BW capability of the I/O channel. In this section, the measured results of the insertion loss (S21) parameter are used to determine the suitability of signal transmission using ultra-thin 3-D glass interposers. Based on the modeling results from Chapter 3, the insertion loss of two major channel components presented in this section may be classified into two types, namely, the redistribution layer (RDL) signal lines and through-package-vias (TPVs) based on their channel length.

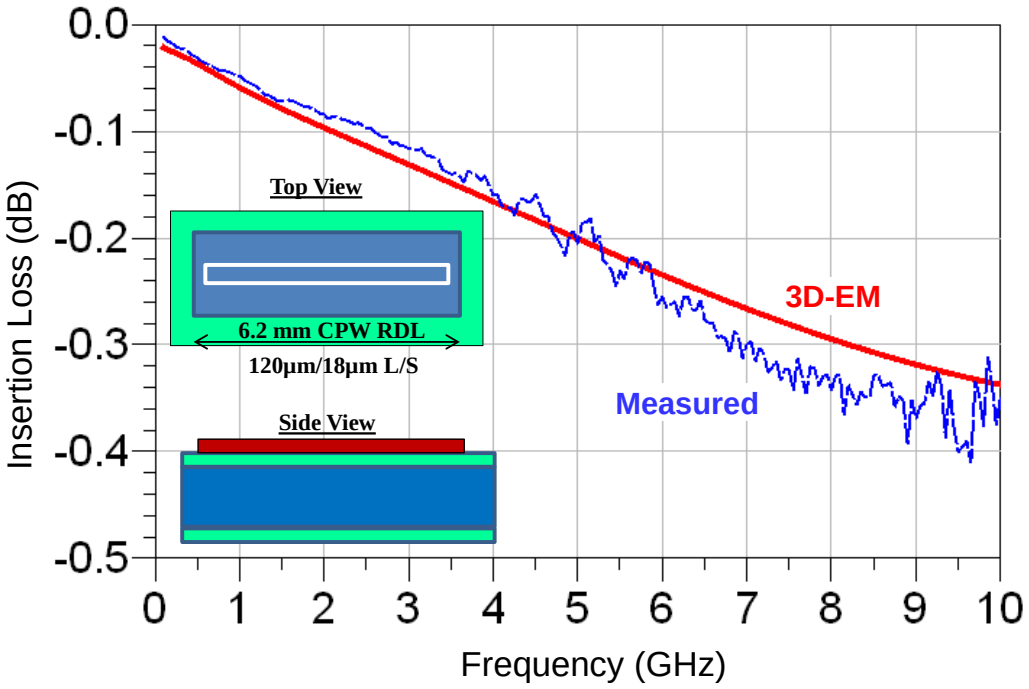


Figure 101: Measured insertion loss (S12) of Glass interposer external I/O traces [25].

Test structures were designed and fabricated to characterize the signal loss through 6.2 mm long coplanar waveguide lines, emulating the typical interconnection lengths of the external I/O channels in 3D glass interposers. The CPW lines on the glass interposer RDL had the lowest loss with 0.06 dB/mm up to 10 GHz due to the ultra-high resistivity of glass, which led to lower substrate loss when compared to silicon interposers. Good correlation was observed between the measured and simulated insertion-loss parameters and these results are summarized in Figure 101.

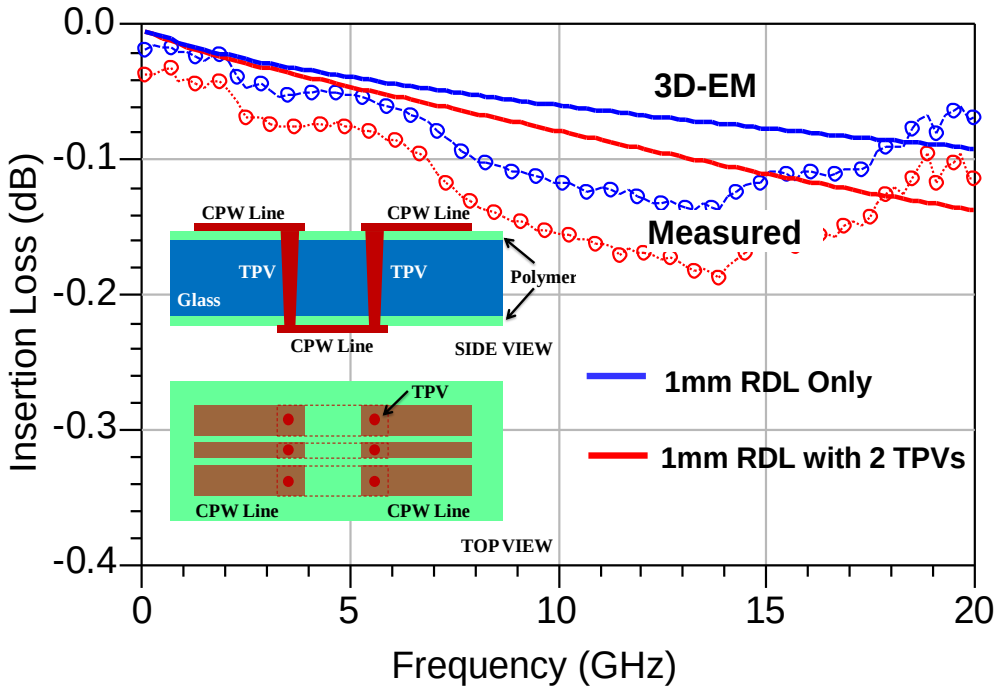


Figure 102: Measured insertion loss (S_{12}) of wide-I/O channel having TPV transitions [25].

The effects of combining signal lines with TPVs were studied to analyze the impact of ultra-small through glass vias on signal performance of the wide-I/O channel. Impedance matched CPW line structures containing 1mm long RDL traces of 120µm line width and 20µm spacing were measured with and without TPV transitions as shown in Figure 102. Minor variations in the measurements were introduced due to the challenges associated with low-loss microwave calibration. The interconnections showed extremely low signal loss (around -0.1 dB) up to 20GHz with good correlation between the measured and simulated insertion loss.

5.4 Summary of Test Vehicle Demonstrations for 3-D Glass interposer packages

- Test vehicles were designed, fabricated, and electrically characterized to demonstrate the feasibility of effective power delivery in 3-D interposer packages using power and ground planes in ultra-thin, glass substrates with small TPVs.

- The self-impedance (Z11) measured at the center of the 17mmx17mm and 10mmx 10mm P/G planes across the 100µm and 30µm-thick glass, respectively, achieved excellent correlation with the simulated results. The mode resonances were in agreement with the proposed analytical equations in Chapter 3.

- The measured 3-D interposer PDN exhibited an overall increase in inductive impedance when compared to the 2-D scenario due to the lateral inductive path. In addition, a new high-impedance peak occurred at 7.4 GHz, which directly correlated with the simulated 3-D glass PDN results. The high-impedance peaks in 3-D PDN were not observed at frequencies below 7 GHz due to the small values of the lateral trace inductances.

- Based on the resonance suppression solutions designed in Chapter 4, the placement and assembly of SMT-type decoupling capacitors on the 3-D glass substrates were studied. Four SMT-type decoupling capacitors (2x1nF and 2x1.2pF) mounted on the top layer of the 100 µm-thick glass interposers were used to demonstrate the effective mitigation of the inductive impedance at the targeted design frequency of 0.4 GHz.

- The insertion loss of both wide-I/O channels and external-I/O channels were characterized with extremely low signal loss (around -0.1 dB) up to 20GHz.

- Therefore, the results from this chapter demonstrate that 3-D glass interposers can be designed with effective power delivery to provide high BW for logic-memory applications.

CHAPTER 6

RESEARCH SUMMARY AND CONCLUSIONS

This dissertation presented one of the first systematic and comprehensive studies to achieve effective power delivery in 3-D glass interposer packages. To overcome the design, thermal, testability and scalability limitations of 3-D stacked ICs with TSVs, a simpler 3D package with double-sided assembly of devices, called the 3-D glass interposer package, was proposed by GT-PRC. This approach achieves high logic-to-memory bandwidth using ultra-thin glass substrates having through-package-vias (TPVs) at the same pitch as TSVs. Such 3-D glass interposer packages have ultra-short, low-loss, and wide-I/O interconnections between the logic device on one side of the ultra-thin glass interposer and memory stack on the other side, thus eliminating the need for complex and costly TSVs in the logic die.

Although using glass as a 3-D interposer has many benefits, this approach introduces fundamental problems in achieving a low-impedance power delivery network due to power-ground resonances, arising from (a) the low-loss property of the glass substrate, and (b) added parasitic inductance due to longer and lateral power delivery path from the printed wiring board (PWB). The data and analysis presented in the previous chapters prove that the objectives of this research were met successfully, leading to the first demonstration of effective PDN design in ultra-thin (30-100μm), and 3-D double-sided glass BGA packages, by suppressing the PDN noise from mode resonances.

A simplified PDN design approach was proposed using a panel-based double-side fabrication process with power-ground planes on 30μm ultra-thin, glass substrates, for potential lower cost and improved electrical performance. Based on this approach, this

dissertation developed three important suppression solutions using, (a) the 3-D interposer package configuration, (b) the selection of embedded and SMT-based decoupling capacitors, and (c) coaxial power-ground planes with TPVs. Finally, the fabrication and assembly of decoupling capacitors on 30-100μm ultra-thin glass test vehicles was performed to demonstrate the measured verification of (a) 3-D glass interposer power delivery network and (b) resonance suppression.

This chapter presents the summary of this dissertation with key contributions and identifies future research directions. A list of the published papers is also provided.

6.1 Research Summary

6.1.1 Modeling and Investigation of Power Delivery Resonances in 3-D glass interposers

- **Electrical Modeling and Simulation of PDN self-impedance**
    - Ultra-thin 30 μm glass substrates with power-ground planes were introduced to minimize the PDN inductance. Multi-port 3D EM models of the die, glass interposer package and PWB were developed and interconnected with lumped parasitics to simulate the PDN self-impedance profile. As a baseline, 2-D glass interposer package structures were modeled having fully-populated 700 ball grid array (BGA) connections with uniform distribution of port locations between the interposer and PWB. In comparison, the 3-D PDN was connected with a much lower number of BGAs (300 pairs) located at the periphery of the glass interposer, due to the placement of the large bottom die.

- The electromagnetic simulations were performed using a dielectric constant for the glass of 5.5 (tan δ=0.006), and 3 μm thick low electrical loss polymer dielectrics on either side of the glass, with a dielectric constant of 3.1 (tan δ=0.002). The loop inductances of the 2-D and 3-D glass interposer package PDN were computed to be 340pH and 440pH, respectively. The results suggested that the high planar capacitance due to the ultra-thin glass interposer resulted in an overall increase (~10-150pH) in the additional loop inductance of 3-D PDN up to 5 GHz. This confirms the additional power delivery requirements of 3-D double-sided glass interposer packages when compared with 2-D glass and organic packages.

- **Analysis of Power delivery network resonances**
  - Full-wave EM models were set up in Ansys-HFSS™ to simulate the principle resonance modes in 17x17mm^2 glass substrates, assuming copper power-ground planes having a thickness of 10 μm, and compared with silicon and organic substrates. The effective permittivity (ε_{eff}) of the total glass interposer package was computed including both the glass core and the polymer RDL dielectric materials. The overall permittivity between the power-ground planes was analytically computed to be around 5.0. The resonance modes were tabulated and correlated with the simulated values.
  - The simulation results showed that the 30 μm thick glass interposer had the lowest overall self-impedance (z11) attributed to the lowest separation between the planes across the ultra-thin core. However, the low dielectric loss and high quality factor inherent to the glass substrate resulted in high

magnitude resonances at GHz frequencies when compared to the silicon interposer.

- A 3D-EM HFSS model was also developed to simulate the insertion loss of signal interconnections with glass TPVs for up to 10 GHz and compared in the presence of power delivery resonances. The effects of PDN resonances were predominant in external I/O channels between the chip and PWB. This result is due to the effects of return path discontinuities at package resonant frequencies, which significantly increase the coupling between the signal channels and power-ground planes. The variations in insertion loss values were correlated with the corresponding change in the power-ground plane self-impedance.
- The results proved that the system PDN with on-chip+interposer+PWB elements was dominated by the on-chip PDN capacitance at higher frequencies. However, there were additional resonances observed in the 3-D PDN self-impedance profile near 7.3 GHz, due to the interaction of the increased lateral inductance with the package cavity. Therefore, this effect should be suppressed by using decoupling elements with low-ESL in the power delivery path.

6.1.2 Resonance Suppression Solutions

- **Power-ground plane pairs in dielectric layers**
  - Power-ground planes were designed and simulated across the thin-film dielectric layers to provide low-ESL distributed capacitance very close to the die, without the need for additional space for discrete capacitors. The

power-ground pairs were interconnected across the glass core using parallel through-vias at fine pitch (30µm) with negligible total (~2 pH) parasitic inductances.

- Parametric studies were performed with two types of build-up polymer thicknesses with: (a) 17.5µm ZIF and (b) 5 µm ZIF. Both these variations were 10X more effective in reducing the magnitude of the self-impedance to ~ 1 Ω up to 10 GHz, when compared to the 180 Ω of an equivalent two-metal layer structure. The use of thinner build-up layers (1-5 µm) is recommended to suppress the inductive impedance at higher frequencies due to its lower loop inductance.

- **BGA placement in 3-D Glass packages**
  - Design guidelines were developed to minimize the PDN impedance peaks, by controlling the placement of solder BGA's. Two approaches were considered, with the split die 3-D configuration (13Ω) resulting in higher suppression of the PDN self-impedance peak than the approach of increasing the BGA pitch of the 3-D glass interposer package (31Ω). These results suggest that the routing of the lateral trace inductance has a much larger impact on the PDN design of 3-D interposers, when compared to the equivalent inductance of parallel BGA's.

- **Embedded Decoupling capacitors within Glass substrates**
  - Embedded decoupling capacitors using ultra-thin integrated passive devices (IPDs) or thin-film technologies were studied to provide effective

high-frequency decoupling, due to the land-side capacitor placement restrictions in 3-D interposers.

- A signal and power integrity tool (SI-wave) was used to simulate the self-impedance profile, including the decoupling capacitors and mounting pads. When compared to similar SMT-based technology, the embedded decoupling capacitors (12x1nF) in 3-D glass interposers provided higher amounts of reduction in the magnitude of the impedance peaks from 8Ω to 0.8Ω at 2 GHz.
- Experimental studies were performed to integrate the high density thin-film embedded decoupling capacitor (150nF x 4nos.; ESR=10 mohm; ESL=0.15nH) at different port locations on the glass substrate. The resulting magnitude of PDN self-impedance was reduced by 10X up to a frequency of 2 GHz. However, additional decoupling locations were needed for 3-D interposers to achieve the same order of impedance as equivalent 2-D BGA glass packages due to the added lateral inductance.

- **Coaxial power-ground planes and vias with high-K liners**
  - A simplified electrical circuit model for coaxial power-ground planes and vias was introduced and analyzed to completely suppress PDN resonances upto 10 GHz. Both (a) moderate-k ($\varepsilon_r = 25$) materials such as tantalum oxide with 400 nm thickness and (b) thin-film polymers ($\varepsilon_r = 3.01$) with 1-5 μm thickness, were integrated into the process flow for the glass interposers.

- A 3-D parasitic extractor solver (Q3D) was used to determine the capacitance and loop-inductance of the coaxial TPVs in the 30-100 µm glass. The parametric model was simulated for both liner materials having a target metallization of 5 µm. The 100µm coaxial glass TPVs achieved the highest capacitance per via with 117 pF. This result was due to negligible inductive parasitics from the thin coaxial liner, when compared to thin-film polymer based coaxial TPVs.
- A 3-D HFSS model was used to design a uniform grid distribution of coaxial vias between two plane pairs, based on the results from the parasitic extraction. The results showed that the placement of the coaxial TPVs reduced the 3-D package PDN inductance from 0.44nH to 3pH.
- The experimental results demonstrated that the presence of coaxial liners completely suppressed the power-ground resonances till 20 GHz and improved the overall signal integrity. Therefore, the 30-100µm glass planes with coaxial TPVs having 400nm Tantalum oxide liner are recommended for PDN design in 3-D glass interposers.

6.1.3 Electrical Characterization of PDN resonances and resonance suppression

- The 3-D glass interposer power delivery network resonances were characterized up to 20 GHz and correlated with the electromagnetic simulation results from Chapter 3. In addition, the suppression of these resonances using decoupling capacitors was verified as a key power delivery solution using the design guidelines developed in Chapter 4.

- Two stack-up configurations were fabricated based on (a) a glass core of thickness 100 μm, having four metal layers, and (b) an ultra-thin glass core of thickness 30 μm, having two metal layers. The samples were measured using a vector network analyzer (VNA) with 250μm-pitch ground-signal-ground (GSG) probes. The self-impedance measurement was performed using a two-port PDN technique, after short-open-load-through (SOLT) calibration.
- The measured mode resonances for 17mmx17mm and 10mmx 10mm P/G planes achieved excellent correlation with the analytical equations. The comparison of the 3-D interposer PDN impedance with the 2-D BGA interposer also revealed a high-impedance peak at 7.4 GHz, in agreement with the simulated results.
- The placement and assembly of SMT-type decoupling capacitors on the 3-D glass substrates were studied. Prior to the assembly, the Cu surface was cleaned with nitric acid to remove the native oxide surface and provide a clean and oxide-free surface required for solder wettability. SAC 305 alloy was used as the solder paste with a melting point of 217ºC. Four SMT-type decoupling capacitors (2x1nF and 2x1.2pF) were mounted on the top layer of the 100 μm-thick glass interposer. The measurements after the assembly of decoupling capacitors demonstrated the effective mitigation of the inductive impedance at the targeted design frequency of 0.4 GHz.
- Based on these solutions, the electrical design guidelines for 3-D glass interposers are summarized in Table 15, including individual targeted suppression frequencies and benefits.

6.1.4 Electrical Design Guidelines for PDN solutions

Table 15: Summary of suppression techniques for 3-D glass interposers

Resonance Suppression Solution	Advantages	Disadvantages	PDN Metric	
			Design Frequency	PDN Inductance at 2 GHz
3-D PDN	N/A	High impedance (180 ohm) peaks at GHz frequencies	N/A	400 pH
P/G plane pairs on dielectric layers	10-50 X impedance reduction across wide frequency band	Increased package layer count	0.1 GHz – 4 GHz	47pH
3-D PDN with increased BGA Pitch (same number of BGAs as 2-D PDN)	2X lower magnitude of high-impedance peak	More expensive package due to finer BGA and PWB compatibility	5-9 GHz	350pH
Split Die 3-D PDN (same number of BGAs as 3-D PDN)	Elimination of high-impedance peaks at high frequencies	Die level changes needed	5-9 GHz	308pH
SMT-based Decoupling	Low cost	Large ESL, No land-side placement on double-side interposers	Few Hz to 0.5 GHz	N/A
Embedded Decoupling capacitors	Can be placed under the die for optimal resonance suppression	Higher cost than SMT-based decoupling capacitors	0.1 GHz – 4 GHz	69pH
Coaxial P/G with High-K dielectric	Lowest impedance with 1000X improvement over 2-D glass substrates	Newer process and High Cost	0.1 GHz – 10 GHz	3 pH

6.2 Key Contributions

The key contributions and novelty of this dissertation can be summarized as follows:

- First study and demonstration of power delivery resonances and suppression in double-sided Glass BGA packages with ultra-small TPVs in glass at same dimensions as TSVs, to achieve high logic-to-memory bandwidth having improved power and signal integrity.

- First fundamental investigation of power delivery resonances in 3-D glass BGA packages with the introduction of power-ground planes on 30μm ultra-thin, glass substrates

    - The primary resonance mechanisms arising in double-sided BGA glass packages were identified using electrical modeling and correlated with existing analytical equations
    - Electrical simulations were used to quantify the small overall PDN inductance increase in 3-D glass interposers when compared to 2-D glass BGAs. This result was achieved due to the high capacitance effect in ultra-thin glass planes.
    - The mechanism of signal-to-power coupling in 3-D interposers due to power-ground resonances and return path discontinuity was studied and demonstrated.
    - Parametric studies provided design guidelines for both 2-D and 3-D glass interposer packages to achieve high I/O BW

- First design and demonstration of resonance suppression solutions in 3-D glass BGA packages
    - Fundamental investigation of resonances mechanisms for multiple power-ground pairs across dielectric layers were performed
    - Design guidelines for embedded capacitors and IPDs in 3-D glass PDN were developed
    - Coaxial power-ground planes and TPVs for resonance suppression with high dielectric liners were introduced and studied in detail.

- First design and characterization of power and signal delivery in 3-D ultra-thin glass interposers with TPVs and RDLs
    - The first measurement of 2-D and 3-D glass power delivery network self-impedance was demonstrated
    - Panel-based double-side fabrication processes were developed in 3-D glass substrates for potential lower cost and improved electrical performance, including assembly optimization for SMT-components
    - First measurements were demonstrated to verify 3-D glass interposer resonance suppression using decoupling capacitors with 100μm ultra-thin glass test vehicles.

6.3 Future Research Directions

The objective of this study was to model, design and demonstrate power delivery resonance suppression in ultra-thin 3-D glass interposer packages to achieve high logic-to-memory bandwidth. Beyond the focus of this thesis, there are a number of topics that can be investigated to achieve improved 3-D glass interposer packages in the future. The first topic can focus on the double-side assembly of dies with fine pitch TPVs in ultra-thin glass substrates and the associated process and thermo-mechanical reliability challenges. This research will help achieve mechanical reliability for the double-sided package, leading to practical applications for 3-D glass interposers. This includes the studies of both chip level and board level interconnections. Materials, processes and assembly conditions can be investigated thoroughly to develop manufacturing compatible methods. The thermo-mechanical reliability of the interconnections should also be studied with focus on the warpage, especially for large size glass substrates. Another critical research topic could be the extension of 3-D interposers to multiple dies for high performance applications. In such hybrid systems with both lateral and vertical interconnection channels, the signal coupling and power delivery challenges can be optimized using active voltage regulators within the glass substrate. IPDs and other embedded functional materials in glass can be used to form such elements for enhanced system performance. The co-simulation of electrical and thermal aspects of 3-D packages can also be an important focus area for these large-scale logic-memory systems.

6.4 Publications

This work resulted in the following peer reviewed journal publications:

6.4.1 Peer-reviewed Journals

1. **Gokul Kumar**, Sitaraman, Srikrishna, Jounghyun Cho, Venkatesh Sundaram, Joungho Kim, Rao R Tummala, "Design and Demonstration of Effective Power Delivery Networks with Suppressed Resonances in Double-sided 3-D Glass Interposer Packages", Components, Packaging and Manufacturing Technology, IEEE Transactions on, 2015 (Accepted)
2. Vijay Sukumaran, **Gokul Kumar,** Koushik Ramachandran, Yuya Suzuki, Kaya Demir, Yoichiro Sato, Toshitake Seki, Venky Sundaram, Rao R. Tummala, "Modeling, Design Fabrication and Characterization of Ultra-thin 3D Glass Interposers with Through Package vias at same pitch as TSVs in Silicon", Components, Packaging and Manufacturing Technology, IEEE Transactions on, Volume: 4, Issue: 5, P-P: 786 - 795, Jan. 2014
3. Qiao Chen, Yuya Suzuki, **Gokul Kumar,** Venkatesh Sundaram, Rao R Tummala, Modeling, Fabrication, and Characterization of Low-Cost and High-Performance Polycrystalline Panel-Based Silicon Interposer With Through Vias and Redistribution Layers," Components, Packaging and Manufacturing Technology, IEEE Transactions on, vol.4, no.12, pp.2035-2041, Dec. 2014
4. Dae Hyun Kim; Athikulwongse, K.; Healy, M.B.; Hossain, M.M.; Moongon Jung; Khorosh, I.; **Gokul Kumar**; Young-Joon Lee; Lewis, D.L.; Tzu-Wei Lin; Chang Liu; Panth, S.; Pathak, M.; Minzhen Ren; Guanhao Shen; Taigon Song;

Dong Hyuk Woo; Xin Zhao; Joungho Kim; Ho Choi; Loh, G.H.; Lee, H.-H.S.; Sung Kyu Lim, Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory), Computers, IEEE Transactions on, Volume: 64, Issue: 1, Pages: 112 – 125, Sept 2013

6.4.2 Conference Proceedings

This work resulted in the following conference publications:

1. **Gokul Kumar**, Raj, P.M. ; Jounghyun Cho ; Gandhi, S. ; Chakraborti, P. ; Sundaram, V. ; Joungho Kim ; Tummala, R., "Coaxial through-package-vias (TPVs) for enhancing power integrity in 3D double-side glass interposers," *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th* , vol., no., pp.541,547, 27-30 May 2014
2. **Gokul Kumar**, Sitaraman, Srikrishna, Jounghyun Cho, Sung Jin Kim, Venkatesh Sundaram, Joungho Kim, Rao R Tummala, "Power delivery network analysis of 3D double-side glass interposers for high bandwidth applications," *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd* , vol., no., pp.1100,1108, 28-31 May 2013
3. **Gokul Kumar**.; Sitaraman, S.; Sridharan, V.; Sankaran, N.; Fuhan Liu; Kumbhat, N.; Nair, V.; Kamgaing, T.; Juskey, F.; Sundaram, V.; Tummala, R., "Modeling and design of an ultra-miniaturized WLAN sub-system with chip-last embedded PA and digital dies," *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd* , vol., no., pp.1015,1022, May 29 2012-June 1 2012
4. **Gokul Kumar**; Bandyopadhyay, T.; Sukumaran, V.; Sundaram, V.; Sung Kyu Lim; Tummala, R., "Ultra-high I/O density glass/silicon interposers for high

bandwidth smart mobile applications," *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st* , vol., no., pp.217,223, May 31 2011-June 3 2011

5. Sundaram, V.; Chen, Q.; Suzuki, Y.; **Gokul Kumar**; Fuhan Liu; Tummala, R., "Low-cost and low-loss 3D silicon interposer for high bandwidth logic-to-memory interconnections without TSV in the logic IC," *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd* , vol., no., pp.292,297, May 29 2012-June 1 2012
6. Tummala, R.R, Sundaram V, Sukumaran V, **Gokul Kumar**, "3D and Low Cost Glass and Silicon Interposer Technologies with TPVs as an Alternative to 3D ICs with TSV," IMAPS 2012
7. Dae Hyun Kim; Athikulwongse, K.; Healy, M.; Hossain, M.; Moongon Jung; Khorosh, I.; **Gokul Kumar**; Young-Joon Lee; Lewis, D.; Tzu-Wei Lin; Chang Liu; Panth, S.; Pathak, M.; Minzhen Ren; Guanhao Shen; Taigon Song; Dong Hyuk Woo; Xin Zhao; Joungho Kim; Ho Choi; Loh, G.; Hsien-Hsin Lee; Sung Kyu Lim, "3D-MAPS: 3D Massively parallel processor with stacked memory," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International* , vol., no., pp.188,190, 19-23 Feb. 2012
8. Natarajan, J.; **Gokul Kumar**.; Sen, S.; Nisar, M.M.; Lee, D.; Chatterjee, A., "Aggressively voltage overscaled adaptive RF systems using error control at the bit and symbol levels," *On-Line Testing Symposium, 2009. IOLTS 2009. 15th IEEE International* , vol., no., pp.249,254, 24-26 June 2009

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